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A Non-blocking Interconnection Network-Shared Cache Organization for Multi-core Processors

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Declaration:

I certify that this thesis submitted for the degree of Master, is the result of my own research, except where otherwise acknowledged, and that this study (or any part of the same) has not been submitted for a higher degree to any other university or institution.

Signed: ……

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Abstract

In modern on-chip multi-core processors and multiprocessor systems, the communication between the processor cores and the shared memory modules of the system, (here in after, the terms ‘shared memory’ and ‘shared cache’ can be used interchangeably), suffers from a bottleneck problem. In the best interconnection network, the crossbar switch, when two or more cores make a request to access the same shared cache module, only one request will be accepted and the other requests have to be honoured in a sequence decided by the arbiter of that module. This increases the latency of the shared variable access. This considerably slows the performance of the cores in executing the program threads and hence, the whole execution process.

In our proposed model for multi-core processor architecture, we have redesigned the shared cache modules and the interconnection network organization. This resulted in a Multi-port Content Addressable Memory (MPCAM) and the bottleneck has been totally eliminated. All the cores of the system can write to and read from this memory simultaneously. The shared variable communication process through this memory, by itself guarantees the snooping cache coherence process automatically. It worth noting that the cache coherence process increases the communication overhead in the current systems. In this organization, there is no queuing, no arbitration, and hence no additional latency. A latency of less than or equal five nanoseconds per shared variable access has been achieved. The simulation results of the MPCAM as part of a multi-core architecture have shown high bandwidth, and negligible cache miss ratio, negligible cache coherence and synchronization overhead as compared to the eight core AMD architecture. At the end of this work, the authors have proposed a linear scalable scheme which expands the system to include large number of cores with

linear growing cost and minimum fixed latency of 1.5t, where t is the MPCAM access time.

Keywords: Multi-core, Multi-threading, Micro-threading, Content Addressable Memory (CAM), Cache Coherence, shared Variables, Interconnection Network, Bottleneck, Contention, Arbitration.

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Chapter 1

Introduction

1.1 Motivation

In shared memory multiprocessor systems, there are three crucial issues to be considered; The interconnection networks and the communication bottleneck problem, the scheduling policy which needs load balancing and true dependency, and the cache coherence problem[Joh07][Chi06][jess96]. All these issues apply equally to the on chip shared memory multi-core processors. Multi-core processors are multiple pipelined processors on a chip. Symmetric shared memory multi-core processors exchange information via shared variables. Shared variables reside in shared memory modules and are accessible by all cores. Accessing the shared memory without delay necessities the existence of efficient interconnection network. Any bottleneck in the network causes delay and hence, degrades the performance of the multiprocessor/multi-core system. Provided that dependence rules are observed in the scheduling policy, the processor needs to read/write the right version of the data. This needs synchronization among the processors through hardware and software cache coherence protocols. Synchronization and cache coherence operations add burden on the communication in the interconnection network. The ideal multiprocessor case occur

when the software perfectly observes the dependence rules and load balancing, and when there is no communication overhead due to the bottleneck in the network and cache coherence operations.

In this thesis we present multi-core architecture to solve the communication among cores and between shared memories, this architecture totally eliminates the bottleneck on the interconnection networks and need for arbitration. It also eliminates the need for cache coherence operations. We can say that, if the program is carefully partitioned and scheduled, it nearly can be executed in time equals to 1/n of the execution time on a single processor, i.e., the speed up of the system is ~n, where n is the number of processors (cores).

1.2 Problem Specification and Justification

Scheduling policy is other problems were migrated from discrete multiprocessor to multi-core processor. Scheduling policy is concerned with dividing program among the processors to be executed in shortest possible time. Scheduling problem will be discussed in next chapter. Scheduling involves partitioning the program into chunks (nodes, grains) and scheduling these chunks to the processors without violating the dependence rules. The nodes have local and shared variable. The local variable is accessible by its node only, whereas the shared variable is accessible by all nodes which need them. Access by number of node must be synchronized so that the node reads or writes the correct version of data. Hardware synchronization and software cache coherence protocols are needed.

All multi-core architecture has distributed cache Level, level1 (L1), level2 (L2) and in some cases level3 (L3) caches which must be coordinated. Multi-core architecture uses

shared caches among the cores. This led us to the last and main problem which is the communication among the cores through accessing shared variables.

In the next chapter we will discussed these two problems; the communication via the interconnection network and the scheduling including the cache coherence operations. Then the proposed architecture will be justified in details. A primary justification is the elimination of these problems and their overhead.

1.3 Thesis Contribution

In modern on-chip multi-core processor systems [Intel12, AMD07, Joh07, Tor10], the communication between the processor cores and the shared cache modules of the system suffers from a bottleneck problem that negatively affects the performance of system. So we proposed a multi-pipelined processor on a chip to solve these problems. In this model we have designed a new interconnection networks based of small cache organization modules that are embedded at the cross points of the crossbar network. It provides a non blocking communication among the cores of the system and the shared memory module including snooping cache coherence at the same time. This organization, i.e., the network plus the dual port CAM (DPCAM) modules, has formed a multiport content addressable memory (MPCAM).

1.4 Thesis Organization

The remaining chapter in this thesis are organized as follows. In the chapter 2, we will discuss the modern multi-core system architecture and analyse its main problems; the contention in the interconnection network, the scheduling policy and the cache coherence. In the chapter 3, we will present the above design, its mathematical model and the results

of its performance as standalone component. In chapter 4, we will display the simulation results within the multi-core architecture and compare it with AMD multi-core architecture. In chapter 5, conclusion and future work will be drawn.