



ABSTRACT

Design of a 16-bit Binary Comparator

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Background: Comparators play a key role in digital circuits by determining the magnitude relationship between binary values. With the need for low-power designs in embedded systems, CMOS technology offers an ideal solution due to its complementary operation of NMOS and PMOS transistors.

Study Purpose/Objectives: This project aims to design a scalable, efficient 16-bit binary comparator using CMOS logic. It targets accurate digital comparison with optimized power consumption, verified through simulation.

Methods: Using Electric VLSI (electricBinary-9.07), we first designed individual logic gates—Inverter, NOR, AND, OR, XNOR—at the transistor level. These gates were used to build a 4-bit comparator, then expanded to 8-bit and finally 16-bit. At each stage, the schematic and layout were tested for logical correctness and electrical performance.

Results: The design yielded accurate comparison results with all three outputs ($A > B$, $A = B$, $A < B$) functioning correctly. Power consumption was significantly lower than that of existing designs, though delay was higher. The hierarchical approach ensured clear signal propagation and modular expansion.

Conclusions: The project demonstrates a complete and functional 16-bit comparator built from the ground up using CMOS gates. Its low power profile makes it ideal for energy-constrained



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systems, with potential for further optimization in delay. The methodology highlights scalability and modular design as key benefits of the CMOS-based approach.

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