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Master Program of Renewable Energy and Sustainability

Finite Control Set – Model Predictive Control of a Nine Level Packed U Cell Grid Connected Multilevel Inverter

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Thesis submitted in partial fulfillment of requirements of the degree

Master of Science in Renewable Energy & Sustainability

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ABSTRACT

This thesis describes a grid-connected Nine Level Packed U Cell (PUC9) topology using a Finite Control Set – Model Predictive Control (FCS-MPC) technique. The proposed system is a single phase multilevel inverter, with four pairs of switches that work in a complementary matter, one DC source and two flying capacitors connected to the grid through a filtering inductor. This topology has the ability to generate nine different voltage levels with less number of active and passive components comparing with conventional multilevel inverter topologies. The proposed control technique (FCS-MPC) aims at reducing the total harmonic distortion (THD) of the grid injected current while balancing the capacitors' voltages at their nominal reference values. Robustness analysis of the proposed model including the effect of a step change in the injected current into the grid, parameters' mismatching, and grid voltage sag and swell have been conducted on a single phase low power (PUC9) inverter. Theoretical analysis, mathematical modelling and simulation results using MATLAB/SIMULINK software are presented in this thesis. The THD of the injected current for the proposed model is 1.13% and the capacitors' voltages error is less than 5%.

التحكم بعاكس متصل بالشبكة ينتج تسعة مستويات مختلفة من الجهد باستخدام نموذج تحكم تنبؤي ذو مجموعة تحكم محدودة

إعداد: علاء صالح أبوقبيطة

ملخص

في هذه الرسالة تم اقتراح طريقة للتحكم بعاكس متصل بالشبكة ينتج تسعة مستويات مختلفة من الجهد باستخدام نموذج تحكم تنبؤي ذو مجموعة تحكم محدودة. النظام المقترح هو عاكس متعدد المستويات أحادي الطور يتكون من أربعة أزواج من المفاتيح تعمل بشكل تكاملي ومصدر جهد مستمر واحد ومواسعين، النظام موصول بالشبكة الكهربائية من خلال محاثة لتصفية اشارة التيار. هذا النموذج من العواكس يمتلك القدرة على انتاج تسعة مستويات من الجهد بأقل عدد من المكونات الفعالة وغير الفعالة مقارنة بالعواكس التقليدية. تقنية التحكم المقترحة تهدف الى تقليل التشوه في اشارة التيار الذي يتم ضخه الى الشبكة ، في الوقت ذاته يحافظ على مستوى الجهد للمواسعات حسب القيمة الاسمية لها. خلال هذه الدراسة تم تحليل متانة النموذج المقترح من خلال دراسة أثر تغيير التيار الذي يتم ضخه الى الشبكة ، وأثر عدم تطابق قيم المكونات المختلفة للنظام مع القيم الاسمية، وأيضا أثر الهبوط والارتفاع في جهد الشبكة. في هذه الرسالة تم تقديم التحليل النظري والنموذج الرياضي وعرض نتائج المحاكاة باستخدام برنامج ماتلاب.

DECLARATION

I declare that the Master Thesis entitled" Finite Control Set – Model Predictive Control of a Nine Level Packed U Cell Grid Connected Multilevel Inverter" is my own original work, and herby certify that unless stated, all work contained within this thesis is my own independent research and has not been submitted for the award of any other degree at any institution, except where due acknowledgement is made in the text.

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DEDICATION

To my Parents ……. For their unlimited support

To my wife ……for her unlimited encouragement and patience

To my Teachers ……..... For help me until the end

To my friends ……. Who give me Positive sentiment

To oppressed people throughout the world and their struggle for social justice and egalitarianism

To our great Palestine

To my supervisor Prof. Sameer Khader

To my brother and friend Dr. Hamza Makhamreh

To all who made this work is possible

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Finally, my ultimate thanks go to the great edifice of science (Palestine Polytechnic University).

TABLE OF CONTENT

LIST OF ABBREVIATIONS

B	Bypassed
C	Charged
CHB	cascaded H-bridge
D	Discharged
DC	Direct Current
EMI	Electro-Magnetic Interference
FC	Flying Capacitor
FCS-MPC	Finite Control Set – Model Predictive Control
Min	Minimized
MLIs	Multilevel Inverters
NPC	Neutral-Point Clamped
PI	Proportional Integral
PLL	Phase Locked Loop
PUC	Packed U Cell
PUC9	Nine Level Packed U Cell
PV	Photovoltaic
PWM	Pulse Width Modulation
S	Switch
THD	Total Harmonic Distortion

LIST OF FIGURES

LIST OF TABLES

CHAPTER ONE
INTRODUCTION

1.1 Background

Nowadays, multilevel inverters (MLIs) are in rapid development and have become a very useful solution for renewable energy resources applications due to its ability to deal with different power rating, switching semiconductors, operating frequency, and applied voltage and current [1].

Many publications have implemented multilevel converter technology and pointed to the importance of using this technology for high-power converters [2].
There are a lot of advantages for multilevel inverters compared to conventional inverters, as stated in table 1.1.

Table 1.1 Comparison between conventional inverter and multilevel inverter [3].

Num.	conventional inverter	multilevel inverter
1	High THD in the output waveform	Low THD in the output waveform
2	Not suitable for high power applications, due to the increased voltage stress on the switches	Used for High power applications.
3	High dv/dt	Low dv/dt
4	High EMI	Low EMI
5	High switching frequency	Lower switching frequency
6	Increased switching losses	Decreased switching losses

A lot of publications have been introduced the most common MLI topologies like Cascaded H-Bridge (CHB), Flying Capacitor(FC), Neutral-Point Clamped(NPC), and Packed U-Cells (PUC) inverters.
PUC inverter (classified as FC inverter) has a lot of advantages compared with other MLI topologies such as:

- High power quality

- The ability and flexibility in the multilayer voltage synthesis
- Simple construction
- Reduced number of switches and DC sources
- Reliability
- Less cost

Due to using one DC source in PUC topology, capacitors voltage have to keep the balance at the reference value, also, the reduced number of switching devices means a reduced number of switching states, so the control strategy plays a vital rule in the inverter performance.

There are many control methods proposed to control PUC inverter, in [4] a novel six band hysteresis controller were proposed, which has a fast dynamic and robust behavior, but it can't deal with variable switching frequency. In [5] the authors proposed a 14-band hysteresis controller to control a 15-level PUC inverter. In [6,7] the authors used two proportional-integral (PI) to control the capacitor voltage at the desired value, and the gate signals were generated using multicarrier and reference voltage comparison.

Model Predictive Control (MPC) is one of control techniques that used for power engineering, in the past, it was not used widely due to high computational cost, but recently, the rapid development in digital signal processors have become the common solution [8-13]. MPC have many features:

- Can be used in a variety of application
- Simplicity
- Effective solution for traditional linear controllers

1.2 Objectives

This thesis aims at propose an appropriate multilevel converter topology and control method using nine level PUC topology and MPC control algorithm that capable to:

- Reduce the total harmonic distortion(THD) in the output waveform by increasing the number of voltage levels
- Reduce the voltage stress on the switches
- Decrease the size of the inverter by reducing the filter size
- Achieve the stability under step change in the injected current to the grid and parameters mismatching

1.3 Methodology

To get the desired results and to achieve the goals of this research, the following steps have been performed:

- Literature review, to understand the issues and problems related to multilevel converters.
- Different models of multilevel inverters related to thesis topic have been simulated using MATLAB/SIMULINK software for analyzing the advantages and disadvantages of those reported technologies.
- Mathematical modeling of the proposed converter topology, in order to select the suitable control technique based on the switching behaviors and related performances.
- Mathematical modeling of the selected control technique(**FCS-**MPC)
- Simulation model using MATLAB/SIMULINK software for the proposed inverter topology.
- Presenting the simulation results.

1.4 Outline of the thesis

In this thesis, nine level PUC (PUC-9) with finite-control-set model predictive control (FCS-MPC) is modeled and simulated. Different loading and parameters change cases have been tested to verify the validity of used approach and to make sure that the objectives have been achieved. A brief outline of the thesis is given below:

- **Chapter one** presents a brief introduction about the thesis title, objectives and methodology to achieve the goals of this research.
- **Chapter two** describes the most common multilevel converter topologies and control techniques with a brief comparisons between these topologies
- **Chapter three** illustrates the mathematical design of the grid, PUC9 inverter topology, and FCS-MPC control technique showing the model prediction, state variables normalization, and calculation of cost function.
- **Chapter four** shows the simulation results using MATLAB/SIMULINK software and the robustness analysis of the proposed model.
- **Chapter five** presents the conclusion of the thesis and proposed tasks for future work.

CHAPTER TWO
MULTILEVEL INVERTER

In this chapter some of most common multilevel inverter should be described, then a brief comparison between them is going to be conducted in order to justify the reasons for choosing PUC inverter topology for our further research. Then detailed analysis for PUC9 topology and its control techniques should be conducted.

2.1 Cascaded H-Bridge Multilevel Inverter

This topology consist of series connected single full bridge inverter, each one has its isolated DC bus, so, almost sinusoidal voltage waveform can be generated. This inverter is transformer less type, and does not need for clamping diodes or flying capacitors [14].

The output voltage levels depending on the number of DC sources, the phase voltage will be able to range from −mVdc to mVdc which would have 2m + 1 levels. Where m is the number of the separate DC sources. By increasing the number of levels, the output voltage waveform becomes nearly sinusoidal, even without using any filter.

This topology can be used for medium and high power applications, and the stress on the switches is less than the regular two level topology since the switch need to withstand only one DC source voltage [15].

The main disadvantages of this topology is the high cost of the inverter, because if we need to increase the number of voltage levels, the number of switches and DC sources must increase significantly.

Figure 2.1 shows the general Cascaded H Bridge multilevel inverter topology. So by increasing the number of the single full bridges, the number of voltage levels is increased.

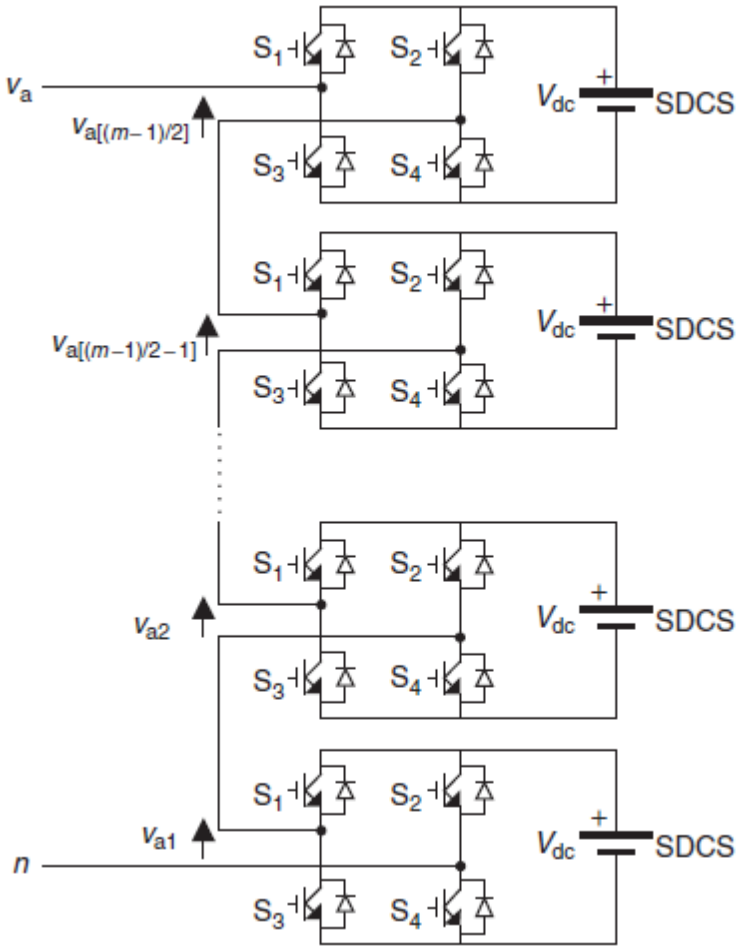


Fig.2. 1: Cascaded H Bridge multilevel inverter topology

2.2 Diode-Clamped Multilevel Inverter

Figure 2.2 shows three and five levels Diode-Clamped Multilevel Inverter topology. The generated voltage Van depends on the shared voltages by the capacitors, and n is chosen as the neutral point. The switches are working in complementary mode (i.e. if S_1 is closed, S_1' is open).

Clamping diodes play an important role in this topology, it is important to clamp the switch voltage at the required value. Table 2.1 presents the switching states for three levels and five levels inverter.

Table 2. 1 Switching states for Diode-Clamped Multilevel Inverter

Van	Three levels		Five levels			
	S1	S2	S1	S2	S3	S4
Vdc/2	1	1	1	1	1	1
Vdc/4	-	-	0	1	1	1
0	0	1	0	0	1	1
-Vdc/4	-	-	0	0	0	1
-Vdc/2	0	0	0	0	0	0

This kind of inverters has some disadvantages, firstly, the clamping diodes have different reverse blocking voltages, secondly, when the number of the voltage levels is very high, the system is impractical to be implemented due to the bulk number of required semiconductors (i.e. the number of clamping diodes can be expressed by (m-1)x(m-2), where m is the number of levels) [16].

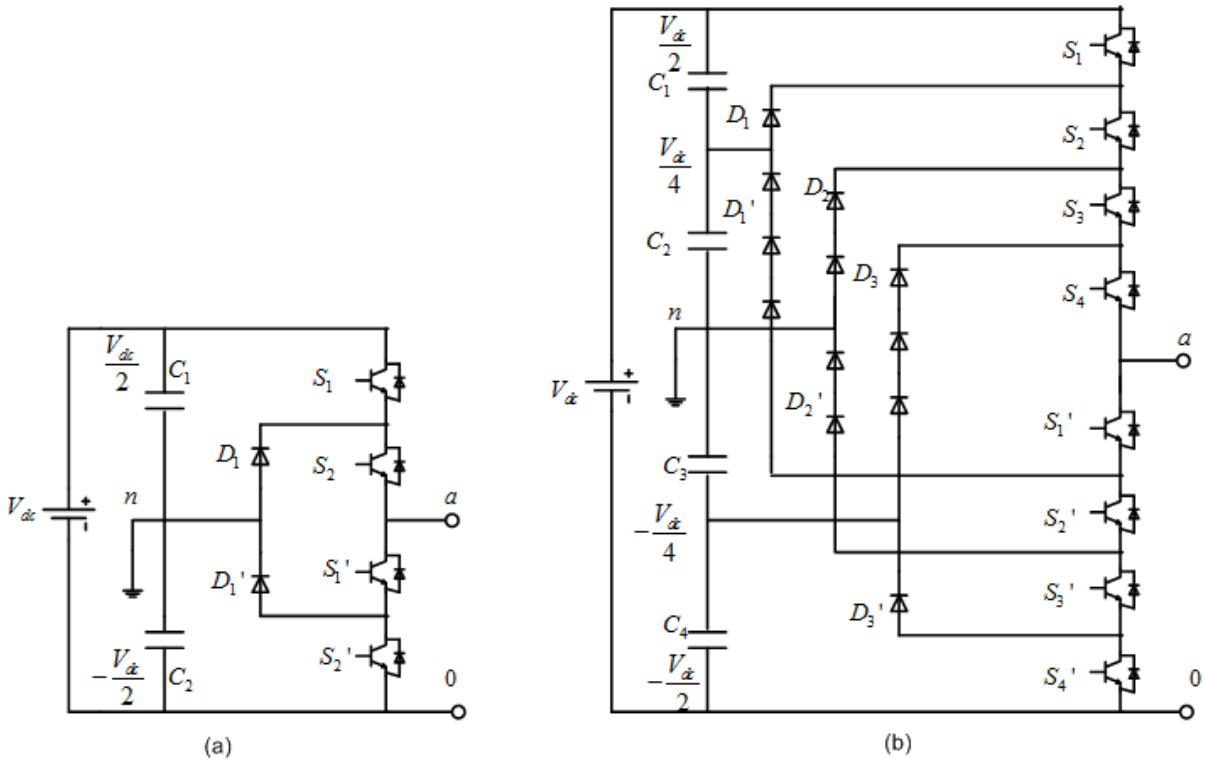


Fig.2. 2: Diode-clamped multilevel inverter topology (a) three levels. (b)Five levels

2.3 Flying Capacitor Multilevel Inverter

This kind of inverters is a replacement for Diode-Clamped Multilevel Inverter, as well shown in Figure 2.3 where three and five levels Flying Capacitor Multilevel Inverter are displayed [17].

The number of switches of this topology is similar to the Diode-Clamped Multilevel Inverter, while the number of the additional capacitors besides the main dc-bus capacitors is (m-1)x(m-2)/2, where m is the number of levels.

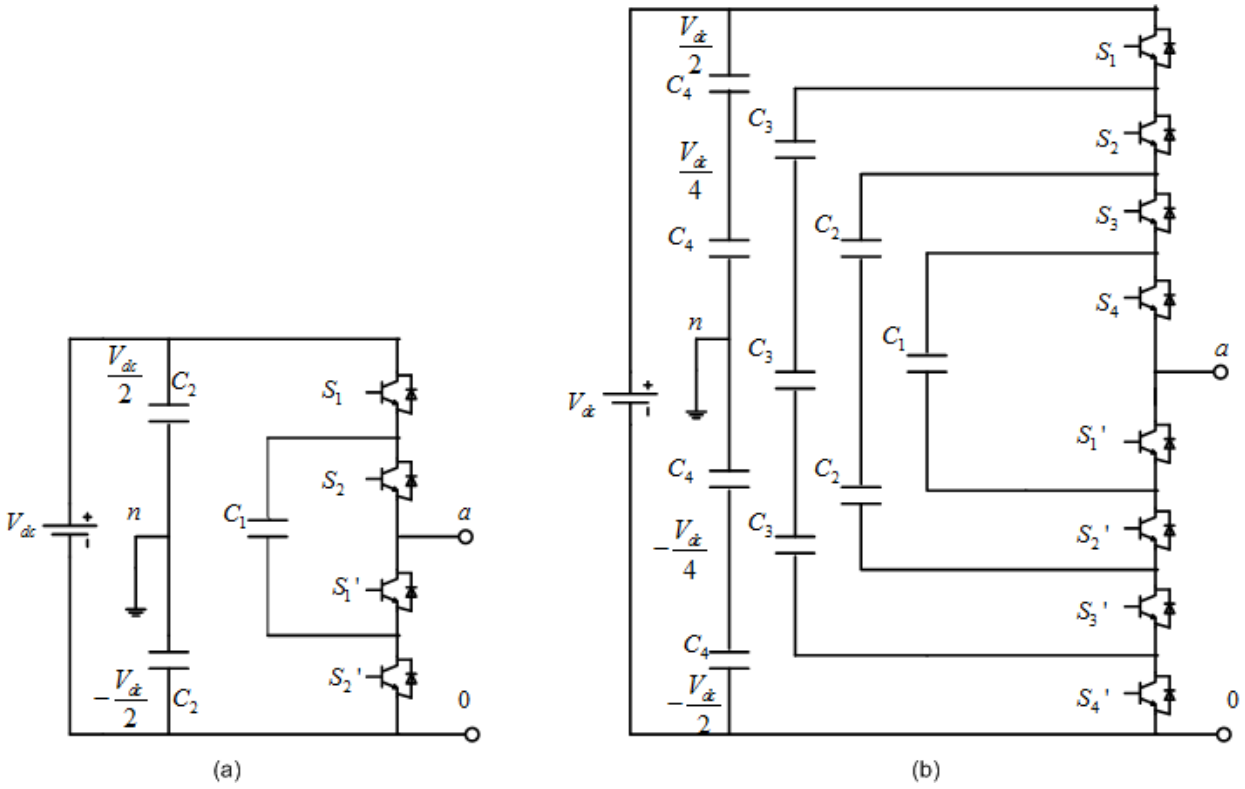


Fig.2. 3: Flying capacitor multilevel inverter topology (a) three levels, (b) five levels

The main advantage of this topology is that it can provide some redundancies for the same output voltage level. This topology has some disadvantages similar to these of Diode-Clamped Multilevel Inverter topology in case of very high voltage levels.

2.4 Packed U Cell (PUC) Multilevel Inverter

This topology consists of six switches and two capacitors placed between these cells as well shown on figure 2.4 for 7-level inverter. In this circuit, V1 represent the DC source generated from photovoltaic (PV) system (using charge controller), and V2 is the voltage of the second capacitor regulated by the control algorithm as mentioned in [1].

The output voltages of this topology are 0, ± V2, ± 2V2, ± 3V2, depending on the switching states. This topology has six switches (S1, S1') , (S2, S2'), (S3, S3') which are controlled in a complementary manner. The switching function is defined using the following logic:

$$Si = \begin{cases} 1, & if\ Si\ is\ ON \\ 0, & if\ Si\ is\ OFF \end{cases} \tag{2.1}$$

Where (i) is the device number with values 1,2, and 3.

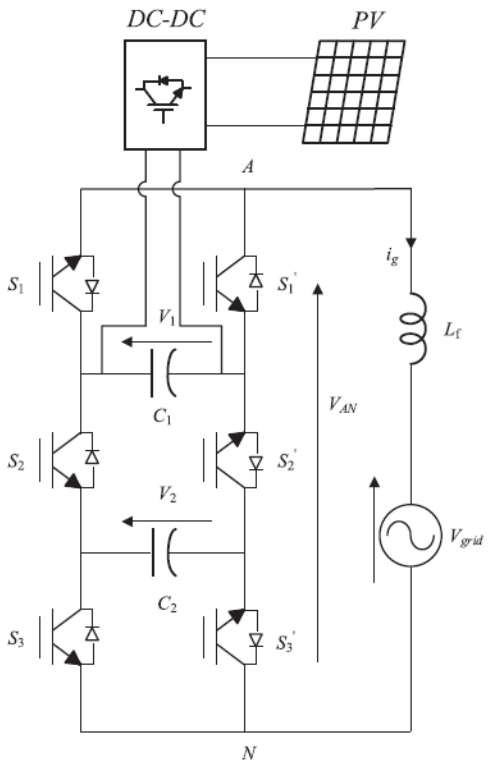


Fig.2. 4: Grid-connected PUC inverter topology with PV power generator

Since, there are three pairs of switches, eight different combination of switching patterns can be obtained as well stated in table 2.2, where the switching table and the capacitors states for 7-level PUC are presented.

Table 2. 2 Switching table and the capacitors states for PUC7 multilevel inverter

State	S1	S2	S3	C1	C2	VAN
1	0	0	0	Bypassed	Bypassed	0
2	0	0	1	Bypassed	Charged	-V2
3	0	1	0	Charged	Discharged	V2-V1
4	0	1	1	Charged	Bypassed	-V1
5	1	0	0	Discharged	Bypassed	V1
6	1	0	1	Discharged	Charged	V1-V2
7	1	1	0	Bypassed	Discharged	V2
8	1	1	1	Bypassed	Bypassed	0

Nine levels PUC inverter (PUC9)

This model is very similar to seven levels PUC inverter, but one pair of switches and one capacitor were added. The THD of the output voltage is decreased due to the generated additional voltage level. Furthermore, the stress on the switches will decrease because the switch handles less value of voltage.

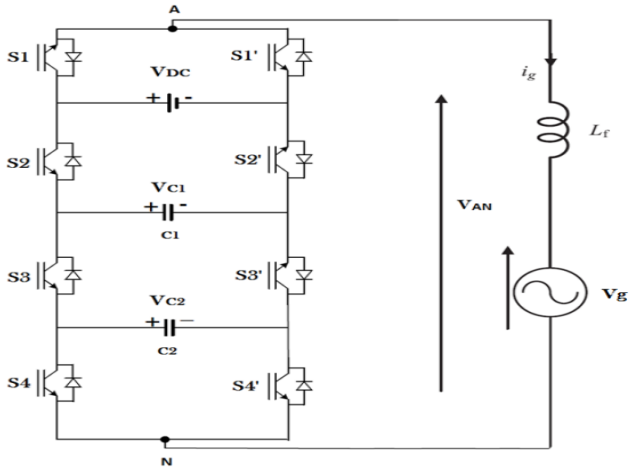


Fig.2. 5: Nine-level PUC multilevel inverter topology.

Comparison between topologies

After the conducted brief descriptions related to multilevel inverter topologies, a short conclusion can be formulated as mentioned in table 2.3 based on comparative analysis. It can be noticed that PUC9 has achieved reliability and less cost compared to the other topologies.

Table 2. 3 Comparison between 9 level inverter topologies

Inverter topology(9 level)	No. of DC sources	No. of capacitors	No. of clamping diodes	No. of switches
CHB	4	0	0	16
NPC	1	8	8	16
FC	1	36	0	16
PUC	1	2	0	8

2.5 Switching Techniques of Multilevel Inverter

Multilevel inverter can be modulated using a lot of switching techniques. The applied switching technique are expected to reduce the switching losses and THD of the output waveform. Having into consideration these constrains, several switching techniques can be applied for multilevel inverters, such as Pulse Width Modulation (PWM), Level-Shifted PWM, Phase-Shifted PWM, Space Vector Modulation, and DC Voltage Balancing [18-21].

Finite Control Set Model Predictive Control (FCS-MPC)

This is one of the most used control techniques that gives an optimal solution for related control problem by calculating the control action at each sampling time. The applied approach uses a dynamic strategy to forecast the future behavior from the current system state. So an optimal control solution will be generated.

The main advantage of this method is that the switching actions are considered as constraints on the control input of the system, as a result for that, the modulation levels are not required [22,23].

Nowadays, MPC is used in several technical control issues [23-27], because it can deal with multivariable control, and unstable systems. However, MPC standard method does not care to the variation range of input and output, which leads to less tracking capabilities.

In general, MPC has the following main components:

1- Prediction model
2- Objective function
3- Optimizing algorithm

In this chapter, the most common multilevel converter topologies and control techniques with a brief comparisons between these topologies are presented, so PUC9 topology and FCS-MPC control technique are selected to achieve the goals of this thesis.

CHAPTER THREE
MODELING OF PUC9 INVERTER TOPOLOGY AND FCS-MPC CONTROL TECHNIQUE

Having into consideration this inverter advantages mentioned in previous chapter, PUC9 is selected as a multilevel inverter topology for this thesis. FCS-MPC control technique is chosen to get the optimized grid-current reference tracking while maintaining the capacitor voltage at its nominal value.

The mathematical model of grid, PUC9 multilevel inverter topology, and FCS-MPC technique are going to be described in this chapter.

3.1 Grid Modelling

The proposed inverter for this thesis is low power single phase inverter connected to low voltage grid with RMS phase voltage (V_g) of 220V at 50Hz and peak voltage (V_{gp}) of 311V.

The grid can be replaced by a concentration elements, source voltage, line inductance and reactance with values stated in table 3.1.

Table 3. 1 Grid parameters

V_g (V)	**V_{gp} (V)**	**Inductance (mH)**	**Resistance (Ω)**	**Frequency (Hz)**
220	311	2.5	0.1	50

3.2 Mathematical Modeling of PUC9 Topology

The proposed model of this thesis has four pairs of switches(S1,S1'), (S2,S2'), (S3,S3'), and (S4,S4') triggered in a complementary matter, let Sx Ɛ{0,1}, where x{1,2,3,4} and the obtained combinations are illustrated on figure 3.1.

$$Sx = \begin{cases} 1, & if\ Sx\ is\ ON \\ 0, & if\ Sx\ is\ OFF \end{cases} \quad (3.1)$$

Where, V_{DC} is the voltage of the single source of the system; V_{C1} is the voltage of the first capacitor; V_{C2} is the voltage of the second capacitor; and V_{AN} is the output voltage of the inverter model.

The proposed model generates 9 voltage levels (0, ±E, ±2E, ±3E, ±4E), where E= $V_{DC}/4$ which presents the reference voltage. The nominal voltage value for V_{DC} = 4E, V_{C1} = 2E and V_{C2} = E

In our model the grid current $i_g(t)$ must track the grid current reference, also the capacitors voltage $V_{C1}(t)$ and $V_{C2}(t)$ must be maintained at their nominal voltage values.

The generated output voltage of this inverter depends on the proposed voltage reference E and on the switching states with values presented in table 3.2.

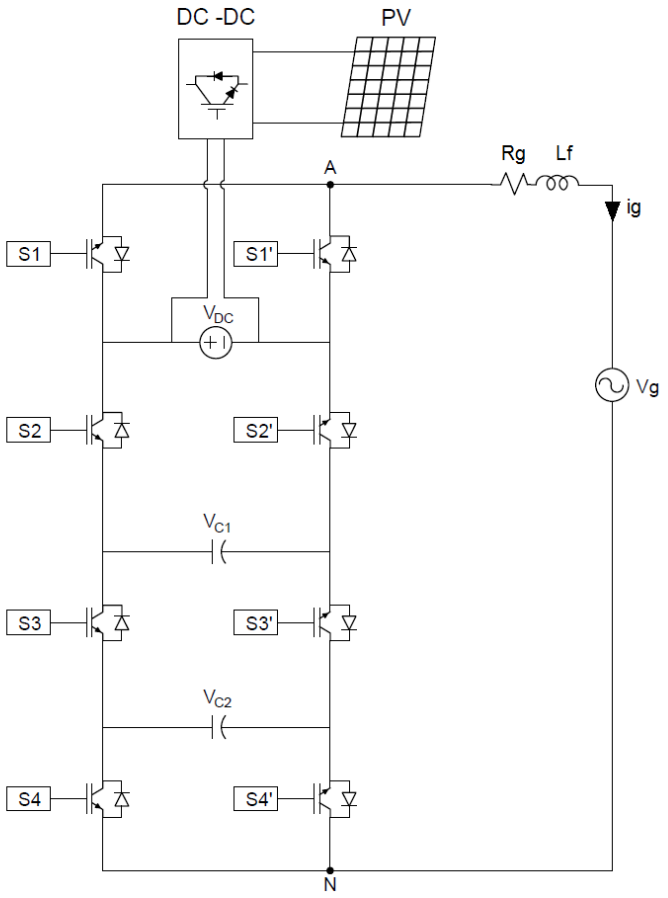


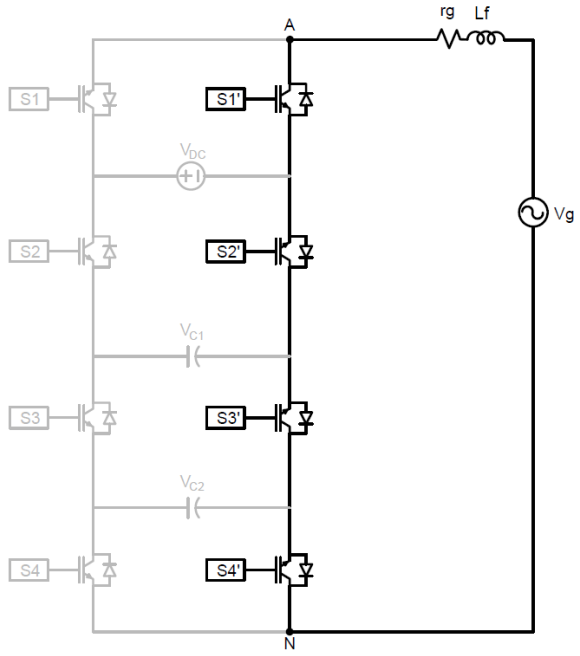
Fig.3. 1: Grid-tied PUC9 multilevel inverter topology

Table 3. 2 The output voltage at various switching combination table and the capacitors' states for PUC9 multilevel inverter

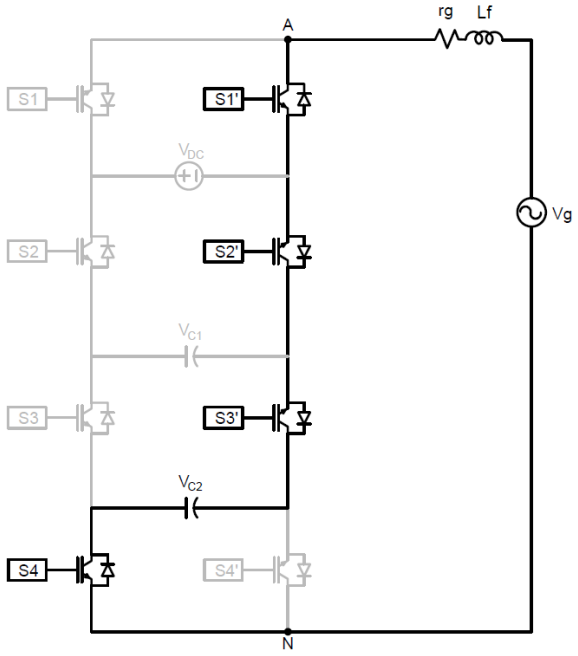
State	S1	S2	S3	S4	Output Voltage	Van	C1	C2
1	**0**	**0**	**0**	**0**	**0**	**0**	**B**	**B**
2	**0**	**0**	**0**	**1**	**-E**	**$-V_{C2}$**	**B**	**C**
3	**0**	**0**	**1**	**0**	**-E**	**$-V_{C1}+V_{C2}$**	**C**	**D**
4	**0**	**0**	**1**	**1**	**-2E**	**$-V_{C1}$**	**C**	**B**
5	**0**	**1**	**0**	**0**	**-2E**	**$-V_{DC}+V_{C1}$**	**D**	**B**
6	**0**	**1**	**0**	**1**	**-3E**	**$-V_{DC}+V_{C1}-V_{C2}$**	**D**	**C**
7	**0**	**1**	**1**	**0**	**-3E**	**$-V_{DC}+V_{C2}$**	**B**	**D**
8	**0**	**1**	**1**	**1**	**-4E**	**$-V_{DC}$**	**B**	**B**
9	**1**	**0**	**0**	**0**	**4E**	**V_{DC}**	**B**	**B**
10	**1**	**0**	**0**	**1**	**3E**	**$V_{DC}-V_{C2}$**	**B**	**C**
11	**1**	**0**	**1**	**0**	**3E**	**$V_{DC}-V_{C1}+V_{C2}$**	**C**	**D**
12	**1**	**0**	**1**	**1**	**2E**	**$V_{DC}-V_{C1}$**	**C**	**B**
13	**1**	**1**	**0**	**0**	**2E**	**V_{C1}**	**D**	**B**
14	**1**	**1**	**0**	**1**	**E**	**$V_{C1}-V_{C2}$**	**D**	**C**
15	**1**	**1**	**1**	**0**	**E**	**V_{C2}**	**B**	**D**
16	**1**	**1**	**1**	**1**	**0**	**0**	**B**	**B**

From table 3.2 it can be stated that, there are twelve redundant states playing a vital role in charging and discharging the capacitors in order to maintain their voltages at the nominal value.

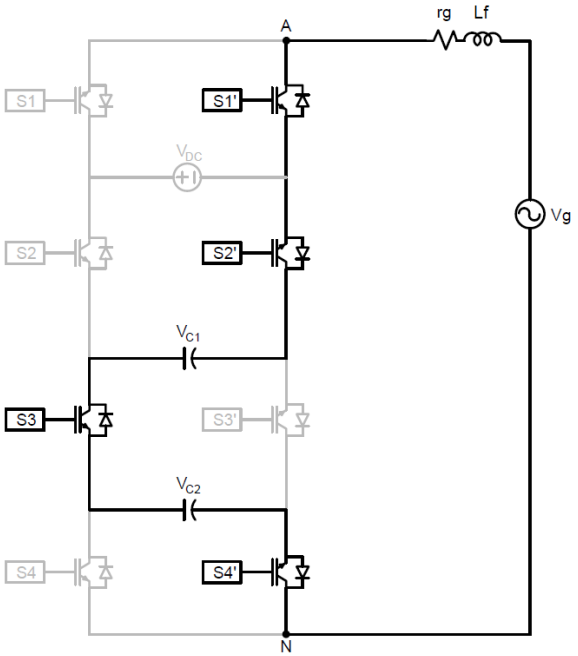
Figure 3.2 illustrate how the output waveform generated for each switching state in a stand-alone configuration.



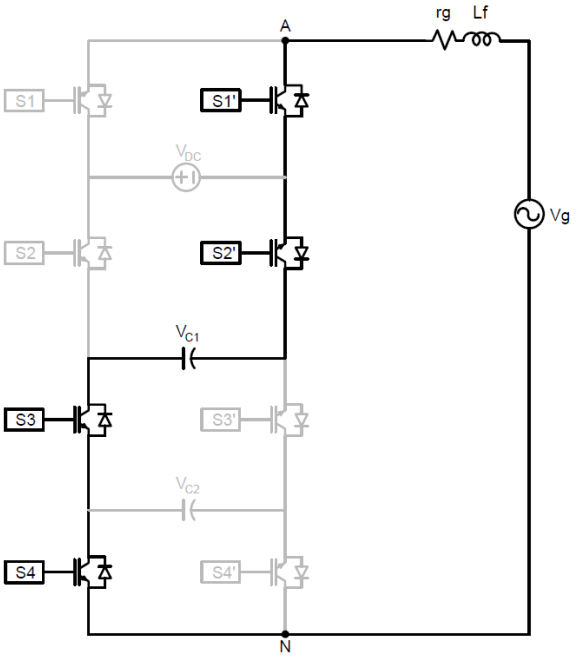
State 1: $V_{AN} = 0$



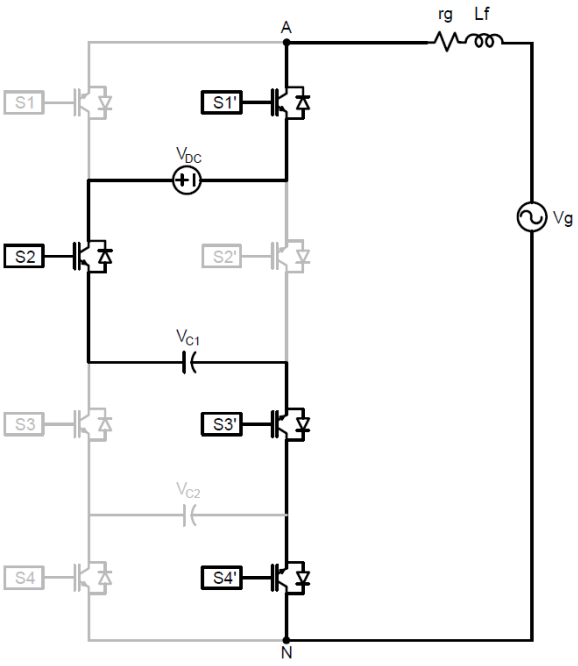
State 2: $V_{AN} = -V_{C2} = -E$



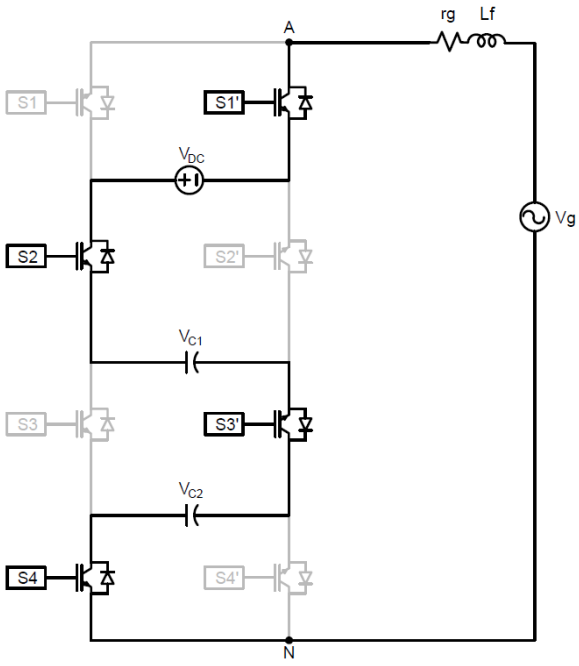
State 3: $V_{AN} = -V_{C1}+V_{C2} = -E$



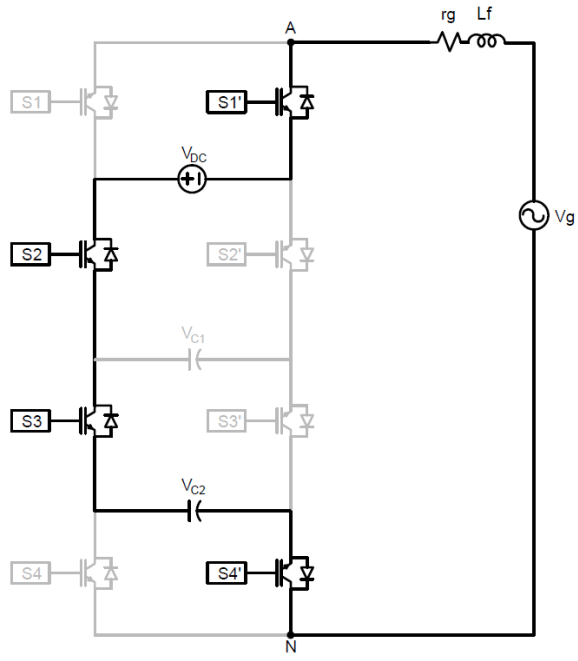
State 4: $V_{AN} = -V_{C1} = -2E$



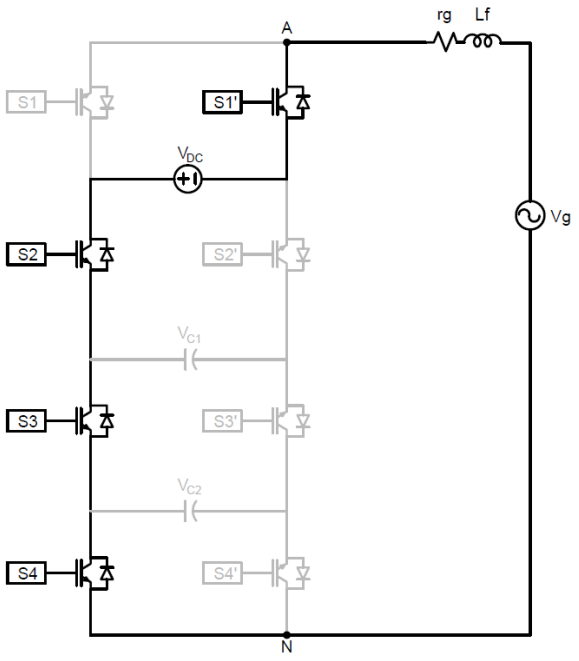
State 5: $V_{AN} = -V_{DC}+V_{C1} = -2E$



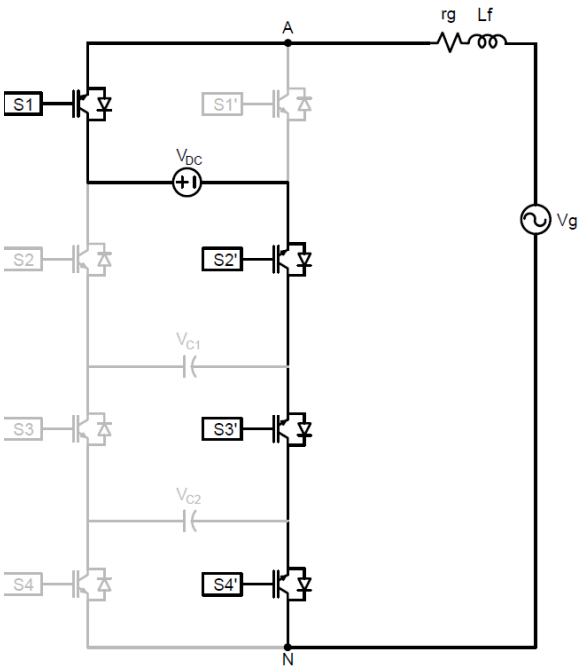
State 6: $V_{AN} = -V_{DC}+V_{C1}-V_{C2} = -3E$



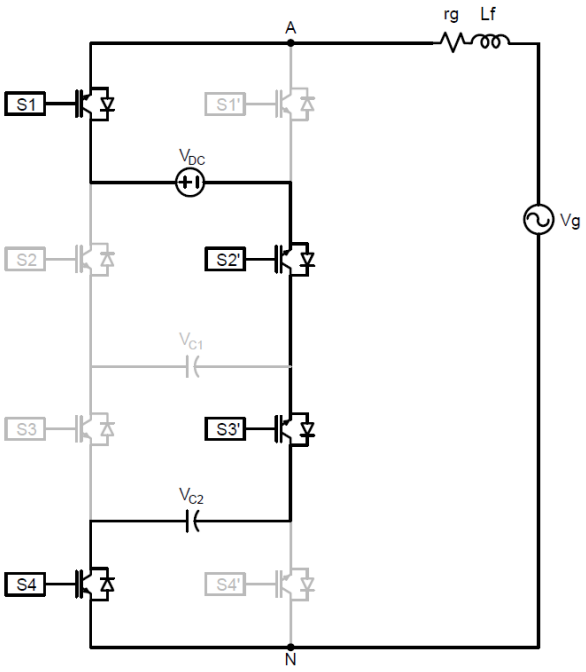
State 7: $V_{AN} = -V_{DC}+V_{C2} = -3E$



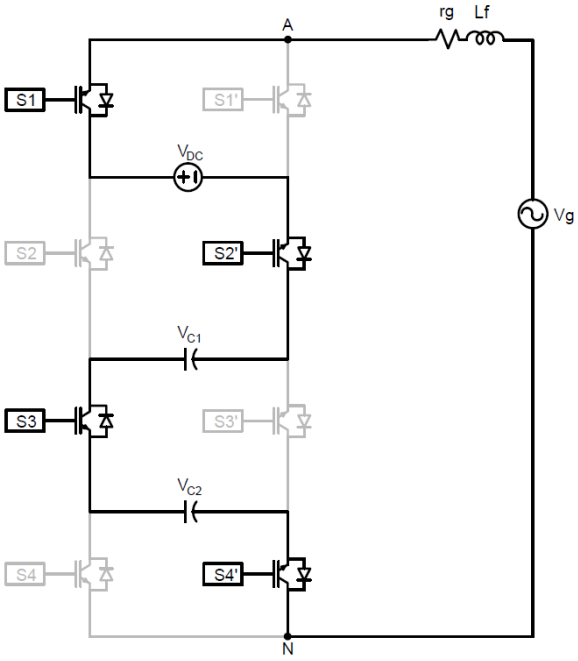
State 8: $V_{AN} = -V_{DC} = -4E$



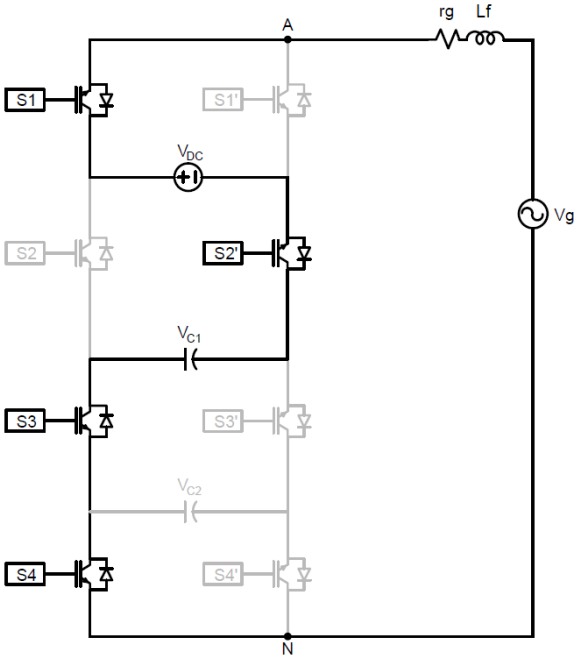
State 9: $V_{AN} = V_{DC} = 4E$



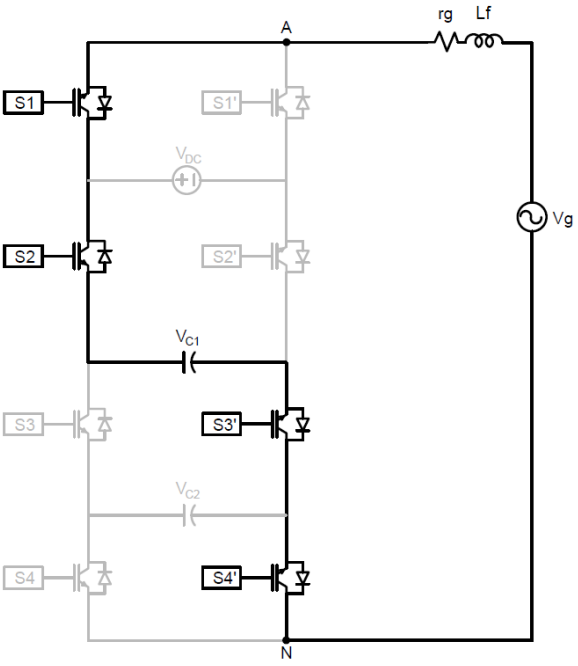
State10: $V_{AN} = V_{DC}-V_{C2} = 3E$



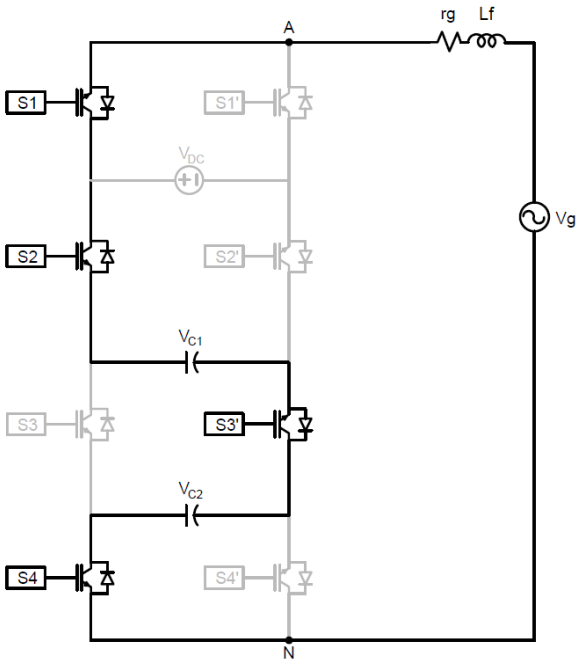
State11:$V_{AN} = V_{DC}-V_{C1}+V_{C2} = 3E$



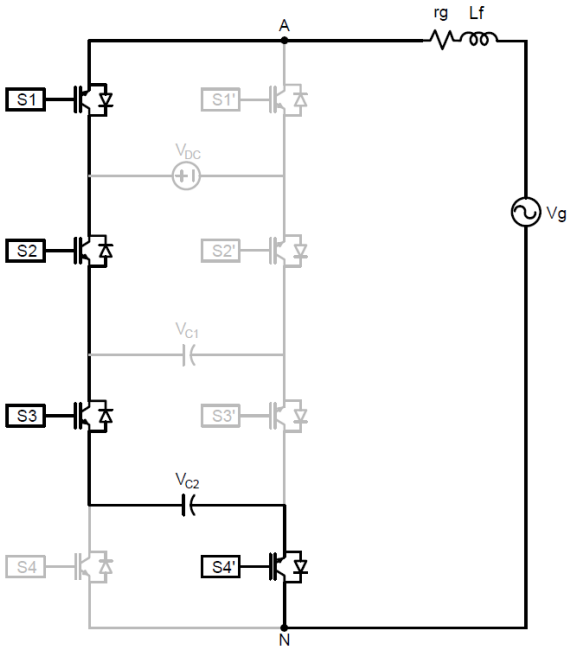
State12:$V_{AN} = V_{DC}-V_{C1} = 2E$



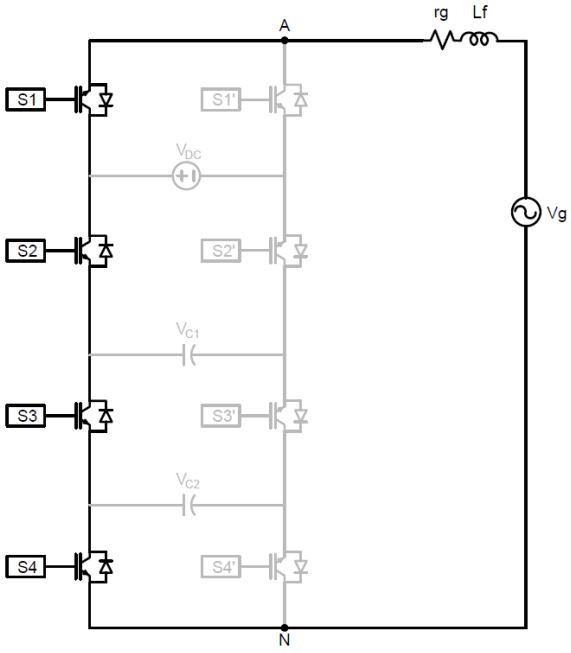
State 13: $V_{AN} = V_{C1} = 2E$



State 14: $V_{AN} = V_{C1}-V_{C2} = E$



State 15: $V_{AN} = V_{C2} = E$



State 16: $V_{AN} = 0$

Fig.3. 2: Switching states model for PUC9

By using Kirchhoff current and voltage laws, relations between grid current $i_g(t)$, capacitors voltages $V_{C1}(t)$ and $V_{C2}(t)$, and the switching states Sx can be expressed as follow:

$$C1\ \frac{dV_{C1}}{dt} = (S3 - S2)\ x\ ig(t) \tag{3.2}$$

$$C2\ \frac{dV_{C2}}{dt} = (S4 - S3)\ x\ ig(t) \tag{3.3}$$

$$Lf\ \frac{dig(t)}{dt} = (S1 - S2)\ x\ V_{DC}(t) + (S2 - S3)\ x\ V_{C1}(t) + \ (S3 - S4)\ x\ V_{C2}(t) - Vg(t) \tag{3.4}$$

Where,

V_{DC}	Source voltage
V_{C1},V_{C2}	Capacitor voltages
S1, S2, S3, S4	Switching states
Lf	Filtering inductance
ig(t)	Grid current
Vg(t)	Grid voltage
C1, C2	Model capacitors

3.3 Mathematical Modeling of FCS-MPC Technique

The main challenge for the control method used in this thesis is to keep the voltages of the capacitors at their nominal voltages while tracking the grid current reference. Another important note, that any change in one of the controlled parameters (such capacitors' voltages and grid current) will affect the others, which in turn complicating the control decisions.

The proposed solution in this thesis is to normalize the state variables by calculating the maximal variations of the state variables. These variations will be used as additional optimization criteria in the cost function calculation.

Model Prediction

The main idea for the control technique of this thesis is to predict the grid current (i_g^{k+1}) and capacitors' voltages (V_{C1}^{k+1}, V_{C2}^{k+1}) for each switching state (voltage vector generated by the inverter) in the means of discrete equations of the system state variables.

In order to simplify the model, the state variables' paths can be considered as rectilinear for a small sampling time. So the state variable that given in equations (3.2),(3.3) and (3.4) will be approximated for each sampling time Ts using the following equation

$$x^{k+1} = x^k + \dot{x}(t).Ts \tag{3.5}$$

Now, the prediction of the state variables at (k+1) sample of time in terms of the recent sample (k) are expressed as follow

$$V_{C1}^{k+1} = V_{C1}^k + (S3 - S2)\frac{Ts}{C1} i_g^k \tag{3.6}$$

$$V_{C2}^{k+1} = V_{C2}^k + (S4 - S3)\frac{Ts}{C2} i_g^k \tag{3.7}$$

$$i_g^{k+1} = i_g^k + (S1 - S2)V_{DC}^k + (S2 - S3)V_{C1}^k + (S3 - S4)V_{C2}^k - V_g^k \tag{3.8}$$

State Variables Normalization

MPC technique does not matter to the variation ranges of the parameters (voltage and current). The main objective of this technique is to reduce the error between the reference and measurement, so it will select the switching state that gives the minimal error.

Before calculating the cost function, this thesis proposes a normalization by calculating the maximal variations of the state variables (ΔV_{C1} max, ΔV_{C2} max and Δi_g max)

$$\Delta V_{C1}max = \frac{2ig}{C1}\,Ts \tag{3.9}$$

$$\Delta V_{C2}max = \frac{2ig}{C2}\,Ts \tag{3.10}$$

$$\Delta i_g max = \frac{V_{AN}}{Lf}\,Ts \tag{3.11}$$

Calculation of Cost Function

The main objective of the cost function is to minimize the difference between the predicted state variables ($V_{C1}^{k+1}, V_{C2}^{k+1}\ and\ i_g^{k+1}$) and there references' values. Thus, the cost function can be expressed as follow

$$g = \left|\frac{V_{C1}^{*} - V_{C1}(k+1)}{\Delta V_{C1}max}\right| + \left|\frac{V_{C2}^{*} - V_{C2}(k+1)}{\Delta V_{C2}max}\right| + \alpha\left|\frac{i_g^{*} - i_g(k+1)}{\Delta i_g max}\right| \tag{3.12}$$

Where V_{C1}^{*} is the nominal voltage of the first capacitor C1 ($V_{C1}^{*} = 2E$), V_{C2}^{*} is the nominal voltage for C2 ($V_{C2}^{*} = E$), i_g^{*} is the reference current and α is the weighting factor that can be adjusted to get the desired results of the model. Fig.3.3 describes the proposed control strategy for PUC9 inverter.

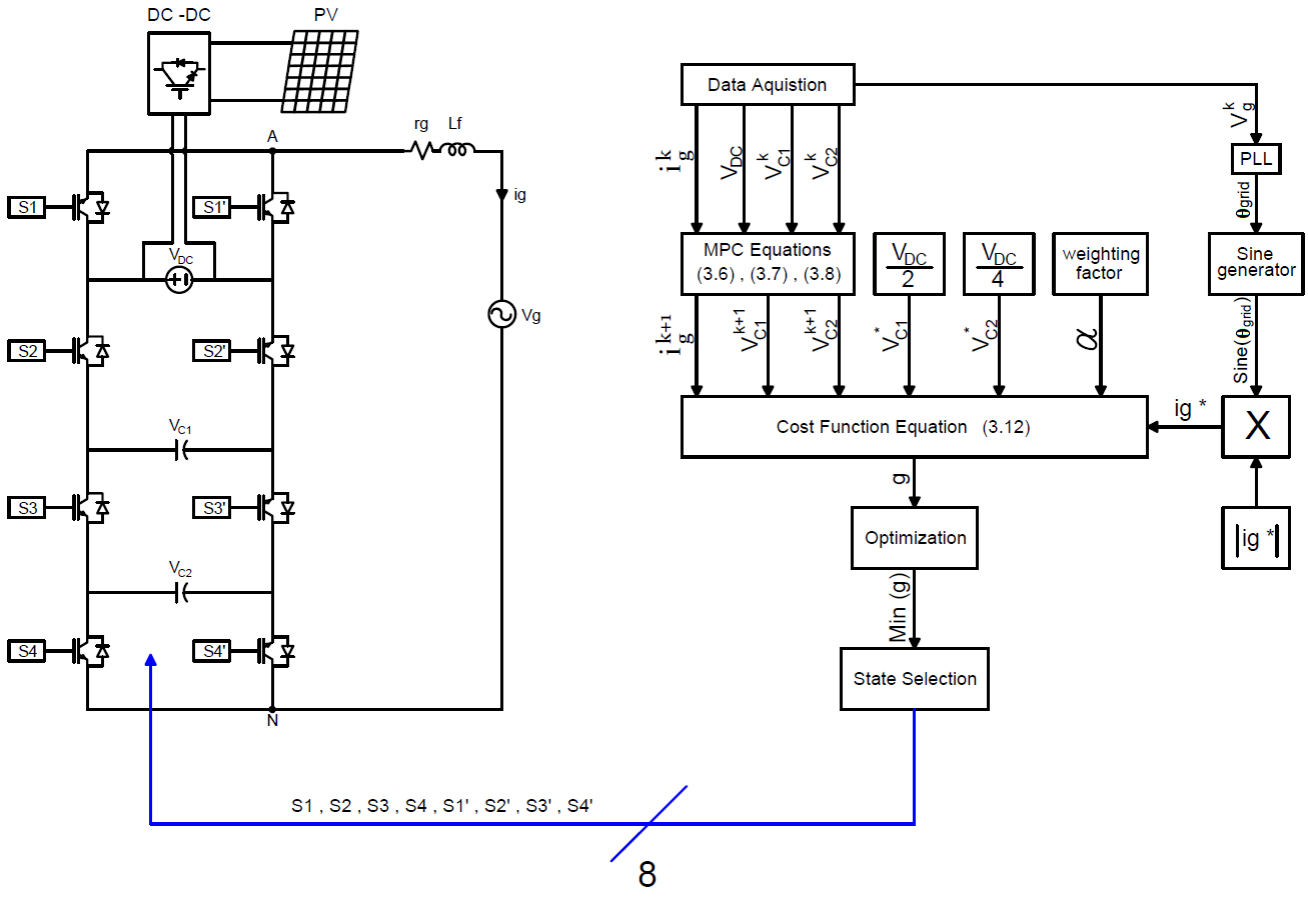


Fig.3. 3 FCS-MPC strategy for PUC9 inverter

Summery

In this chapter, the mathematical model of PUC9 topology and FCS-MPC technique are presented in order to be used in the simulation model to get the desired results.

CHAPTER FOUR
SIMULATION RESULTS

Using MATLAB/SIMULINK software, the performance of the proposed PUC9 inverter topology and FCS-MPC control technique are presented in this chapter. For more details, kindly refer to See appendix A for the Simulink model and appendix B for PUC9 topology model.

4.1 Simulation Parameters Setup Details

Table 4.1 shows the initial parameters for the grid side, filter and inverter of the model.

Table 4. 1 Initial parameters' values for thesis proposed model

parameter	value
Grid-side parameters	
Line to neutral voltage, Vrms, [V]	220
Frequency, f, [Hz]	50
Phase shift, θ, [dg]	0
Filter parameters	
Resistance, rg, [Ω]	0.01
Inductance, Lf, [mH]	2.5
Inverter parameters	
Input DC voltage, V_{DC} , [V]	400
Desired voltage of C1, V_{C1}, [V]	200
Desired voltage of C2, V_{C2}, [V]	100
Capacitance of C1, [mF]	7
Capacitance of C2, [mF]	1
Number of voltage levels, n	9
Sampling time, Ts, [μs]	25
Output rated power, Po, [kW]	5

4.2 Weighting Factor (α) Tuning

Weighting factor plays a vital role in the inverter performance [1], it used to achieve the desired performance and the stability for this proposed model. The tuning of α must be done based on minimizing the total harmonic distortion (THD) of the grid current waveform and the error on the capacitors' voltages (V_{C1} and V_{C2}). Attention to be paid that THD of the grid current, V_{C1} and V_{C2} voltage errors are considered as a performance indicators for α value selection.

Figure. 4.1 illustrate the effect of varying weighting factor (α) on the performance indicators (THD, VC1 and VC2). Note that as α increases VC1 and VC2 error voltage increases, but THD is fluctuating between 3.07% and 1.31%. The optimum value of α is selected based on the minimum value of THD where α=0.22, and THD is moved to of 1.1%, where this value is used for all test cases in this thesis.

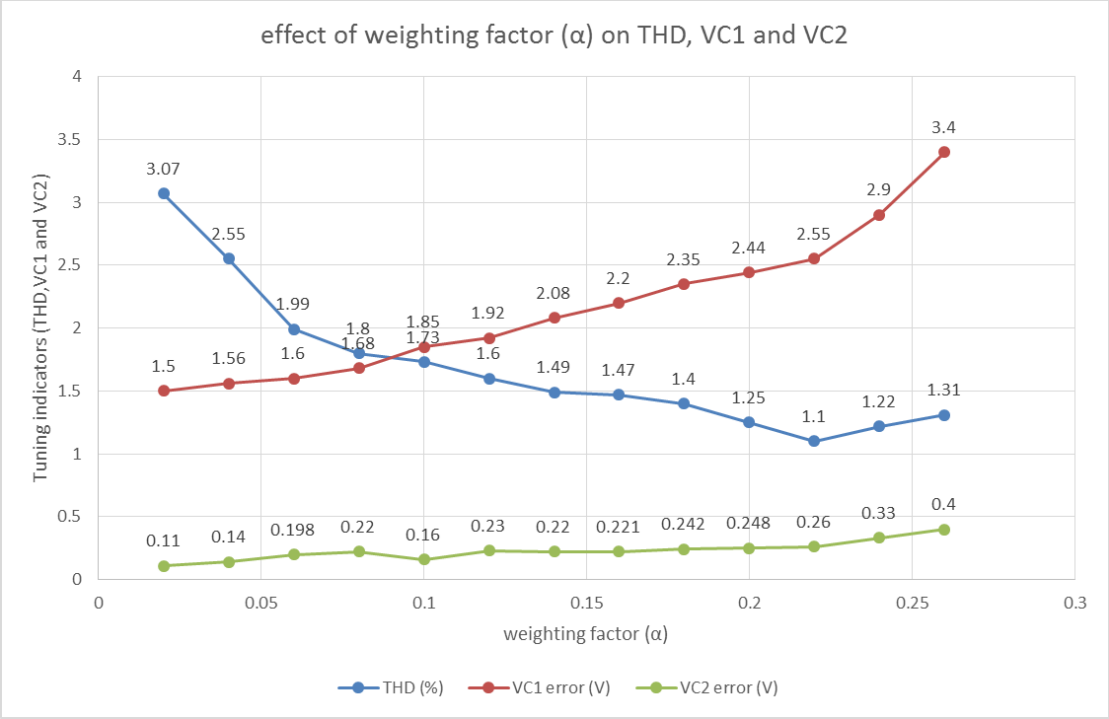


Fig.4. 1: The effect of varying weighting factor (α) on the performance indicators

4.3 Simulation Results for 5kW Power Output

To get the desired results of the proposed model, the output voltage of the inverter Vin must be greater than the grid voltage. Fig 4.2 shows the output voltage of the inverter Vin which has a peak value of 400V, while the grid voltage has a peak value of 311V. . Furthermore, the 9 voltage levels are sequentially illustrated in this figure.

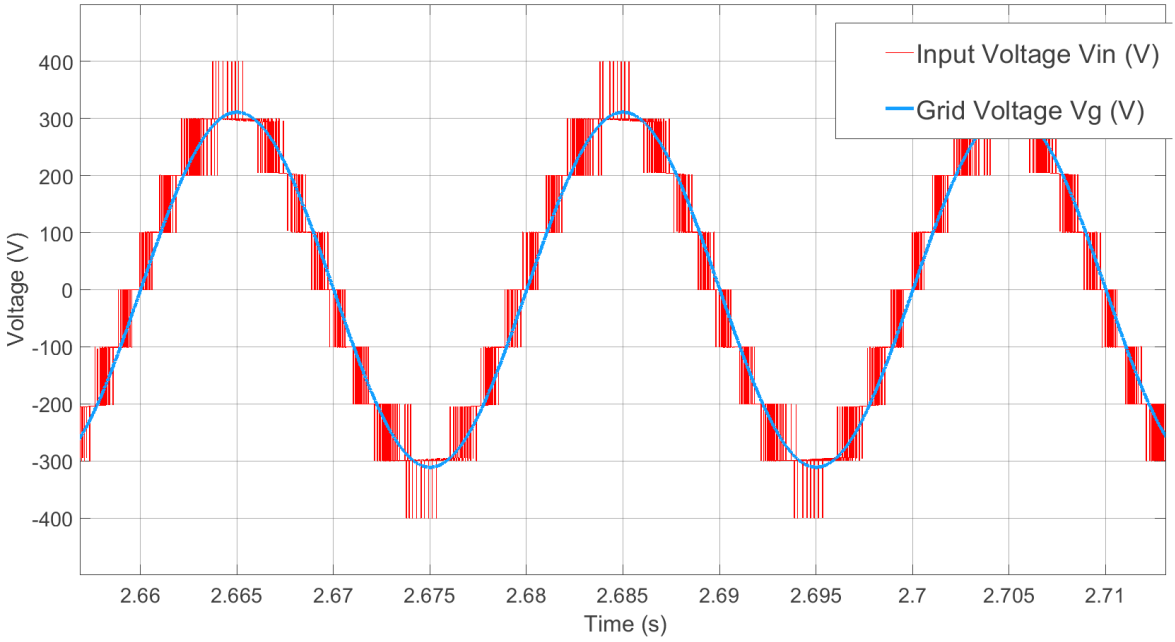


Fig.4. 2: Voltage waveforms of the inverter and the grid

The injected current to the grid ig(t) is shown in Fig.4.3 with values very closed to the reference current value $I_{Gref}(t)$. That means the THD of the current waveform is very small.

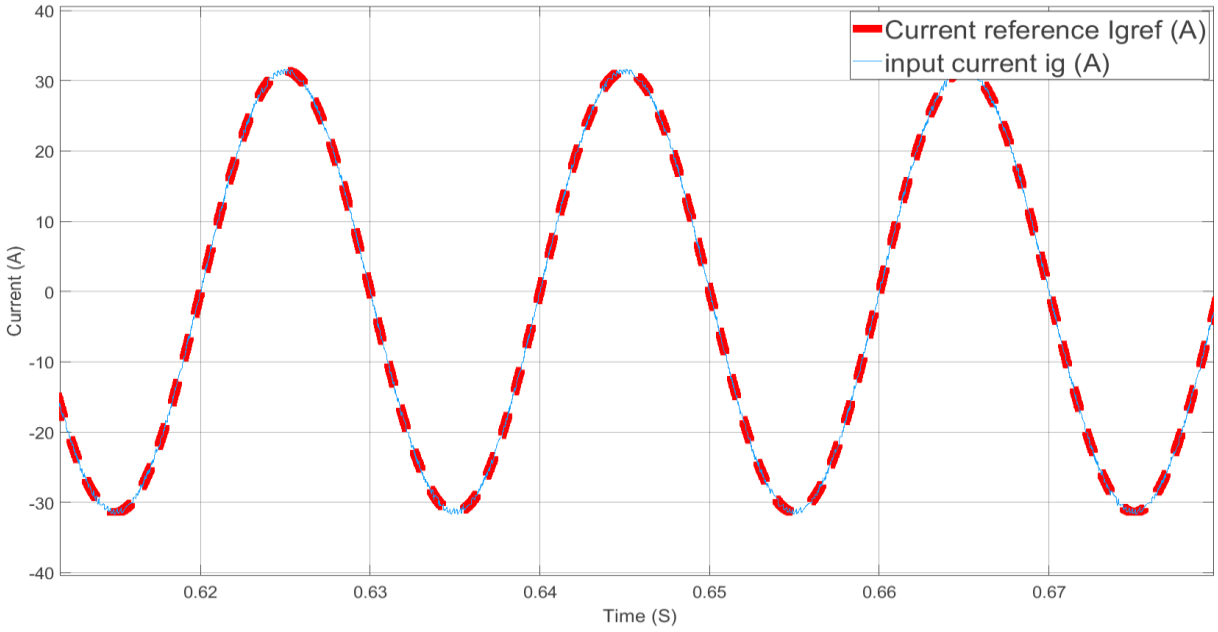


Fig.4. 3: Injected current and reference current waveforms

Figure .4.4 illustrates the capacitors' voltages, where they are controlled as requirement around the reference values (V_{C1}= 2E = 200V and V_{C2} = E = 100V), and the steady state error is relatively small (less than 5%).

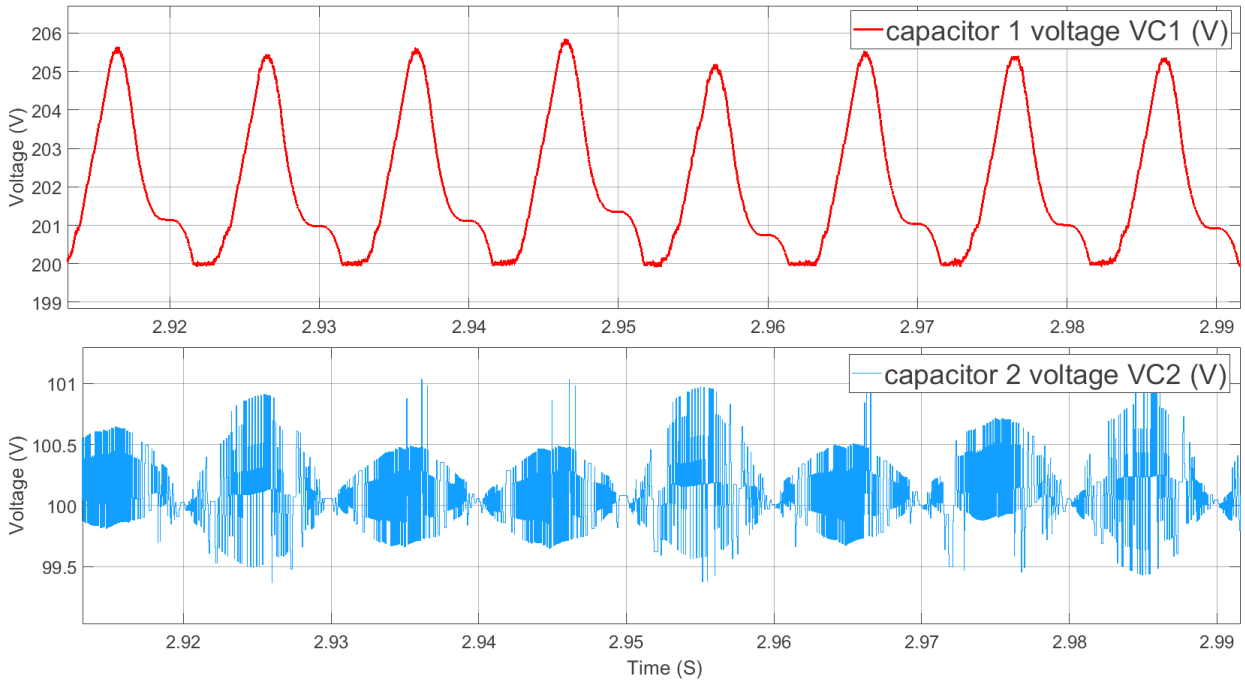


Fig.4. 4: Capacitors' voltage waveforms

Figure 4.5 shows the steady state error of injected current, which is relatively small (less than 5%).

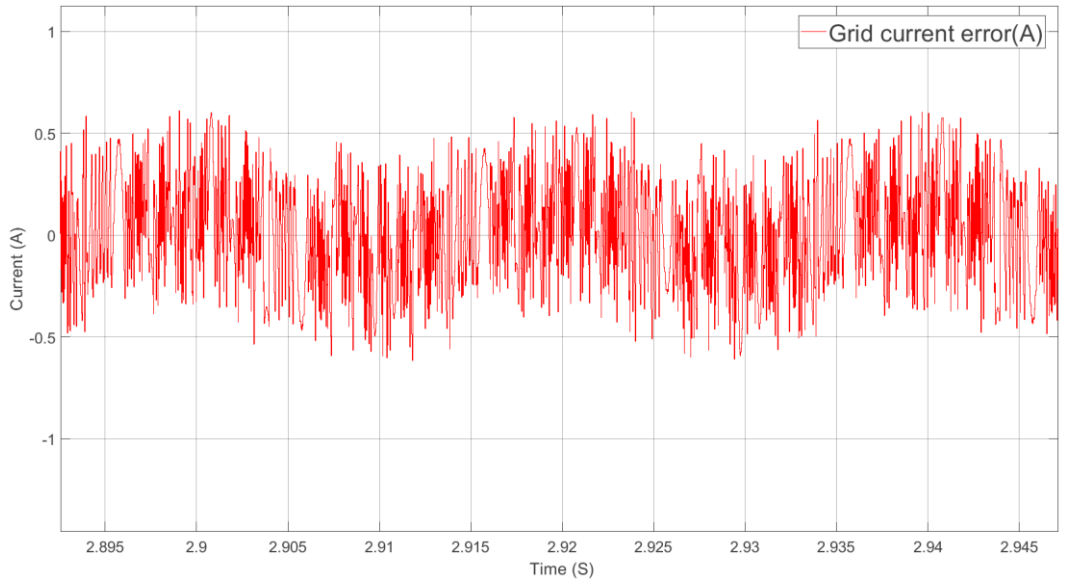


Fig.4. 5: Injected current error

By analyzing the output current waveform, it's clear that the THD is very small (THD=1.13%). See Fig.4.6.

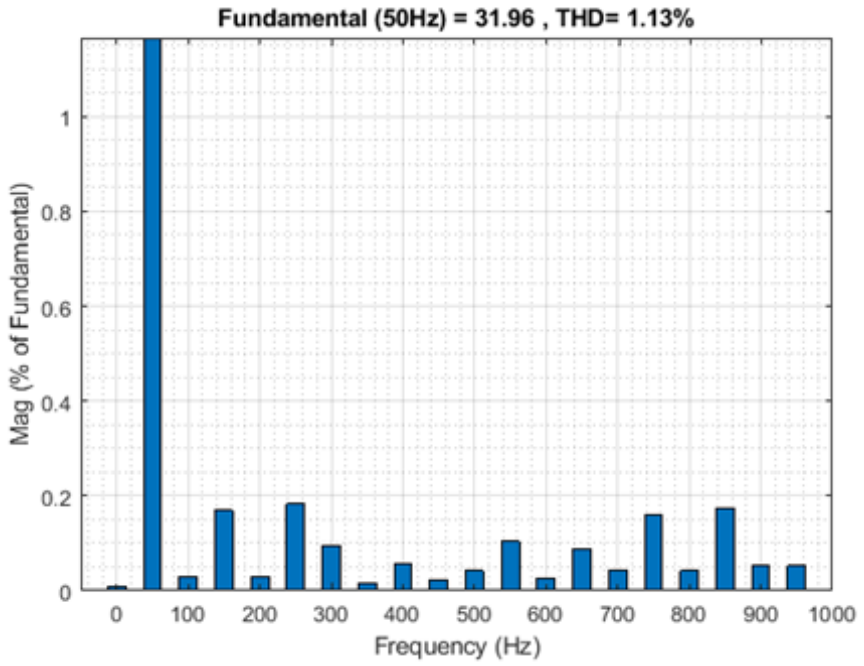


Fig.4. 6 : THD spectrum histogram.

4.4 Step Change in the Output Power of the Inverter

To study the transient operation of the inverter, a step change (at time of 0.525 s) of the injected current (ig) is done, where the current rises from 11.36 A to 22.72A, as shown in Figure 4.7 , where it is clear that the response of the injected current is very fast, the capacitors' voltages error increased slightly but still relatively small (<5%), and the output power of the inverter increased from 2500 W to 5000 W within 1 cycle (0.02 s).

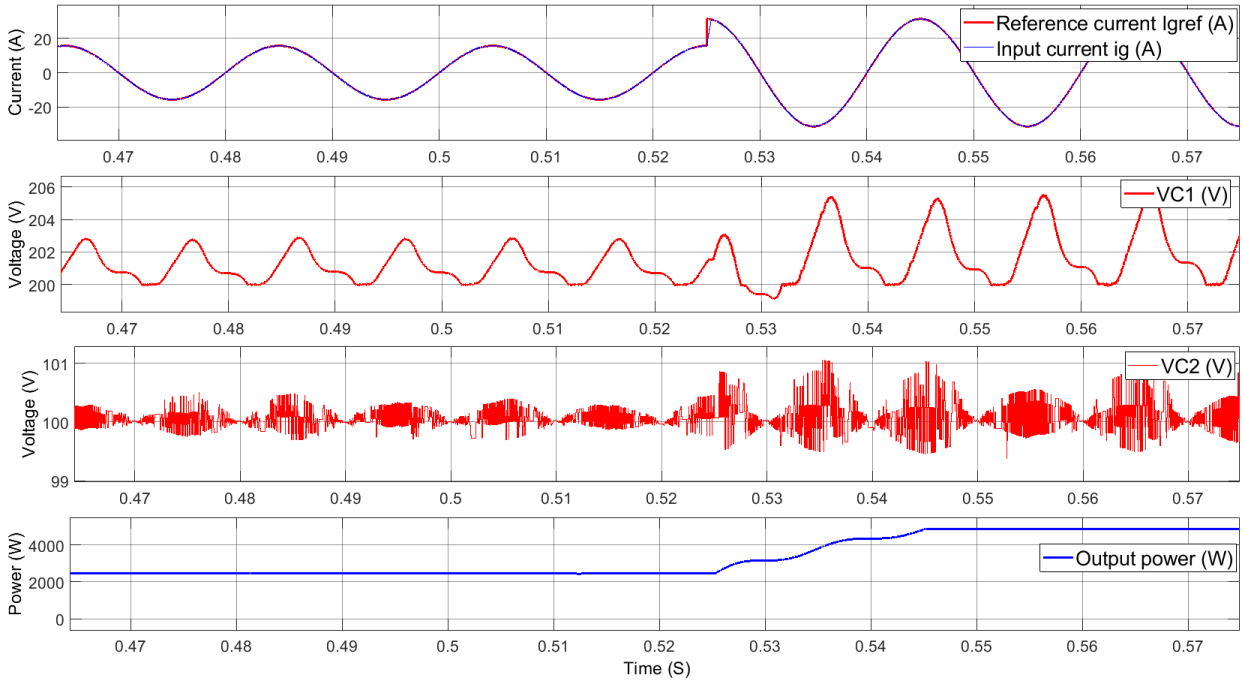


Fig.4. 7: Injected current, VC1, VC2, and output power waveforms during step change in the current

Figure 4.8 shows that the injected current error increased very slightly, but still very small. Also there are no change in the output voltage waveform. See Fig.4.9.

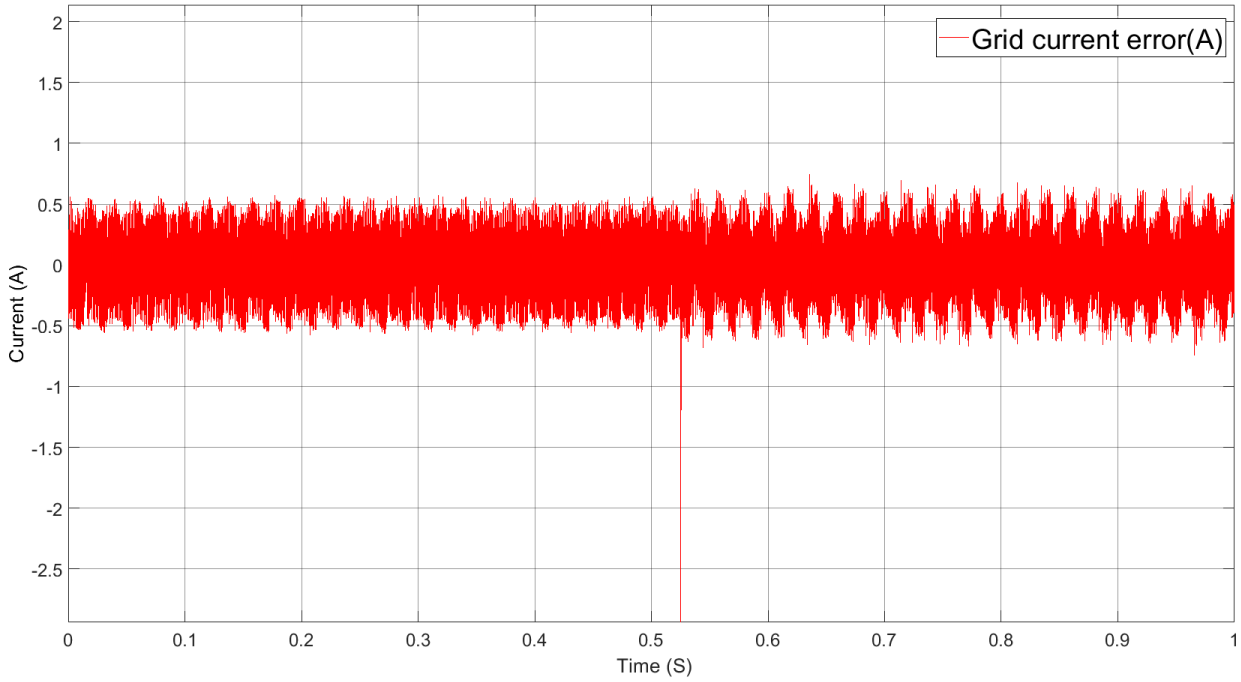


Fig.4. 8: Injected current error during step change in current

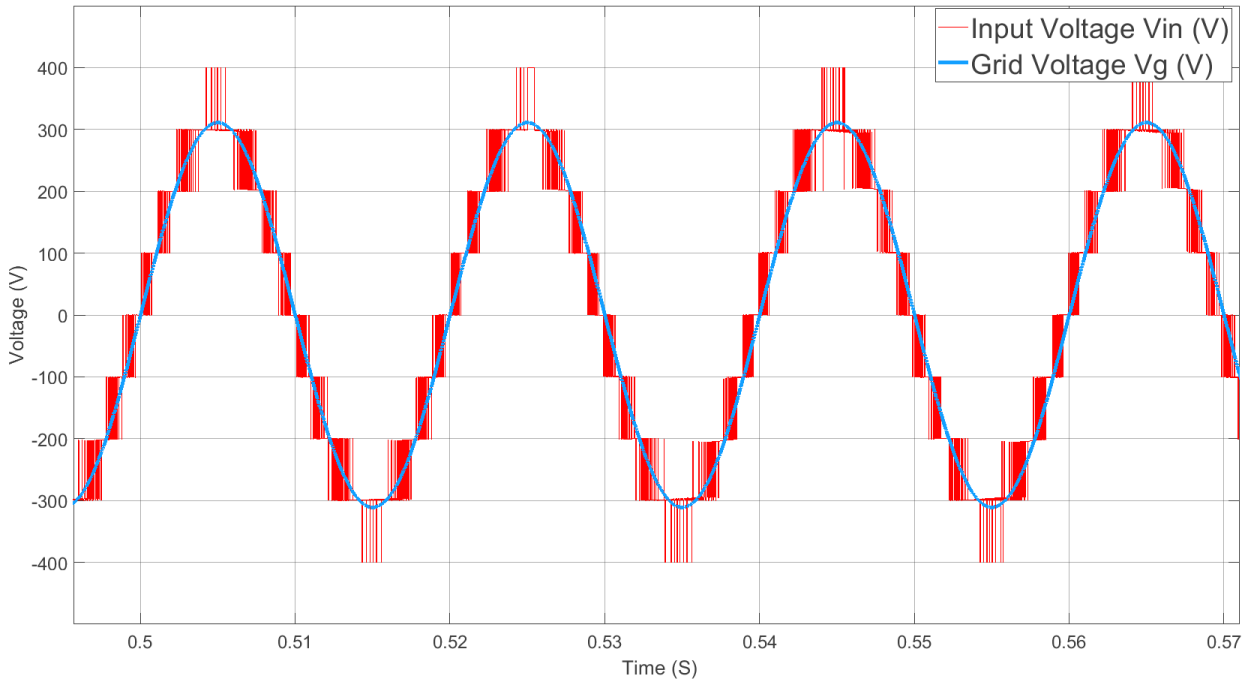


Fig.4. 9: Voltage waveforms of inverter and grid during step change in current

4.5 Robustness Analysis

In order to prove that the proposed model is robust, the model has been simulated under the effect of capacitors (C1, C2) and inductor filter (Lf) mismatches, also grid voltage sag and swell step change. This effect is observed by proposed study by changing the values of C1, C2 and Lf from 50% to 150% of their nominal values, also by changing the grid voltage from 90% to 110% of the rated value.

The Effect of Capacitors and Inductor Mismatches

We note from Fig.4.10 that if the difference of the capacitance of C1 is between -50% to 50%, the THD is fluctuating slightly around 1.1% (but still stable) and ΔV_{C2} also stable around $0.3V_{RMS}$, and there is no significant difference. ΔV_{C1} decreases from 4.9 V_{RMS} to 1.8 V_{RMS}, but, anyway the steady state error is relatively small (less than 5%).

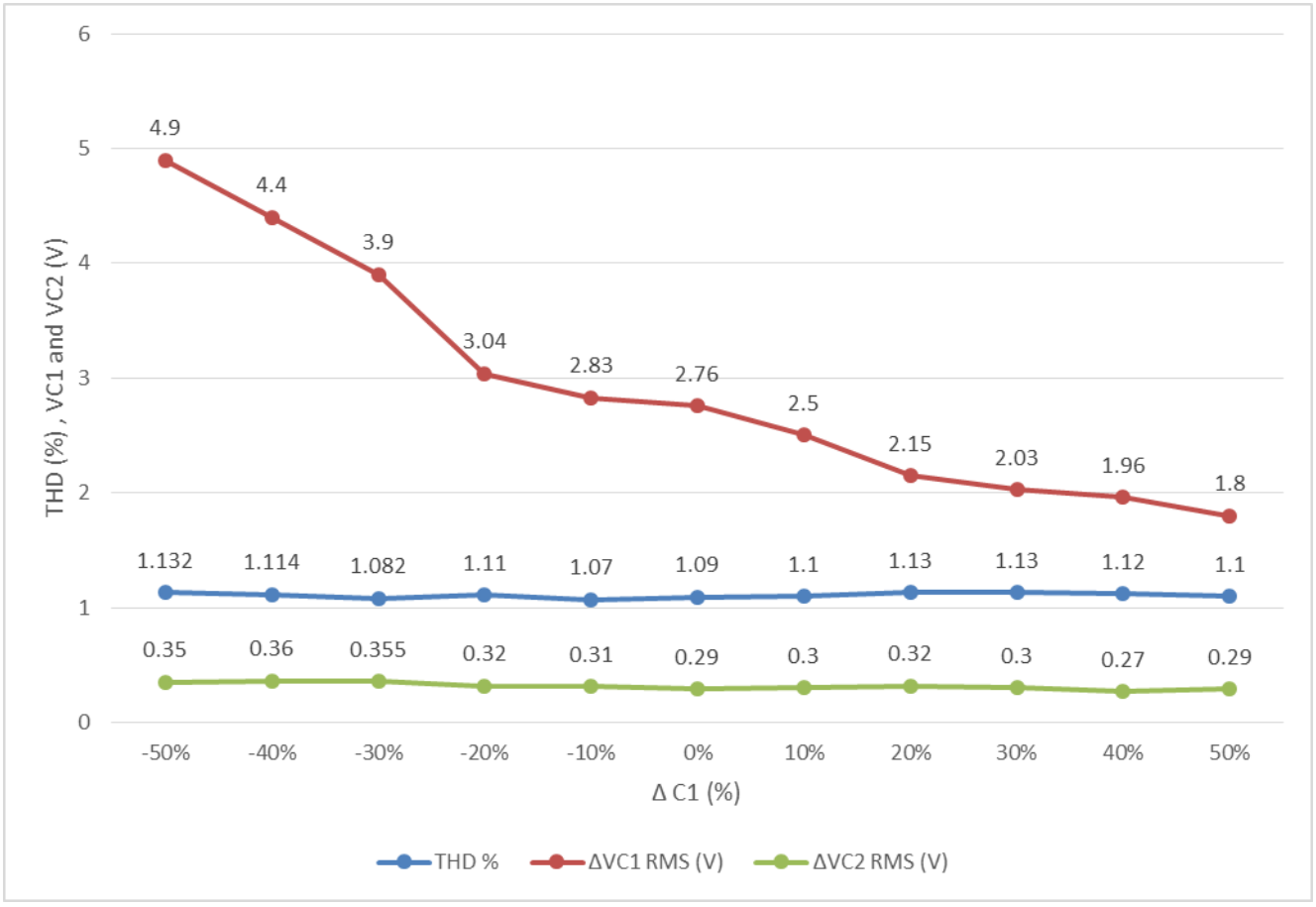


Fig.4. 10: Effect of changing the capacitance of C1 on the performance indicators

Figure 4.11 illustrate that if the change of the capacitance of C2 is between -50% to 50%, the THD is fluctuating slightly around 1.1% (but still stable) and ΔV_{C1} also stable around 2.7V_{RMS} and there is no big difference. ΔV_{C2} is decreasing from 0.51 V_{RMS} to 0.22 V_{RMS}, but, anyway the steady state error stills small (less than 5%).

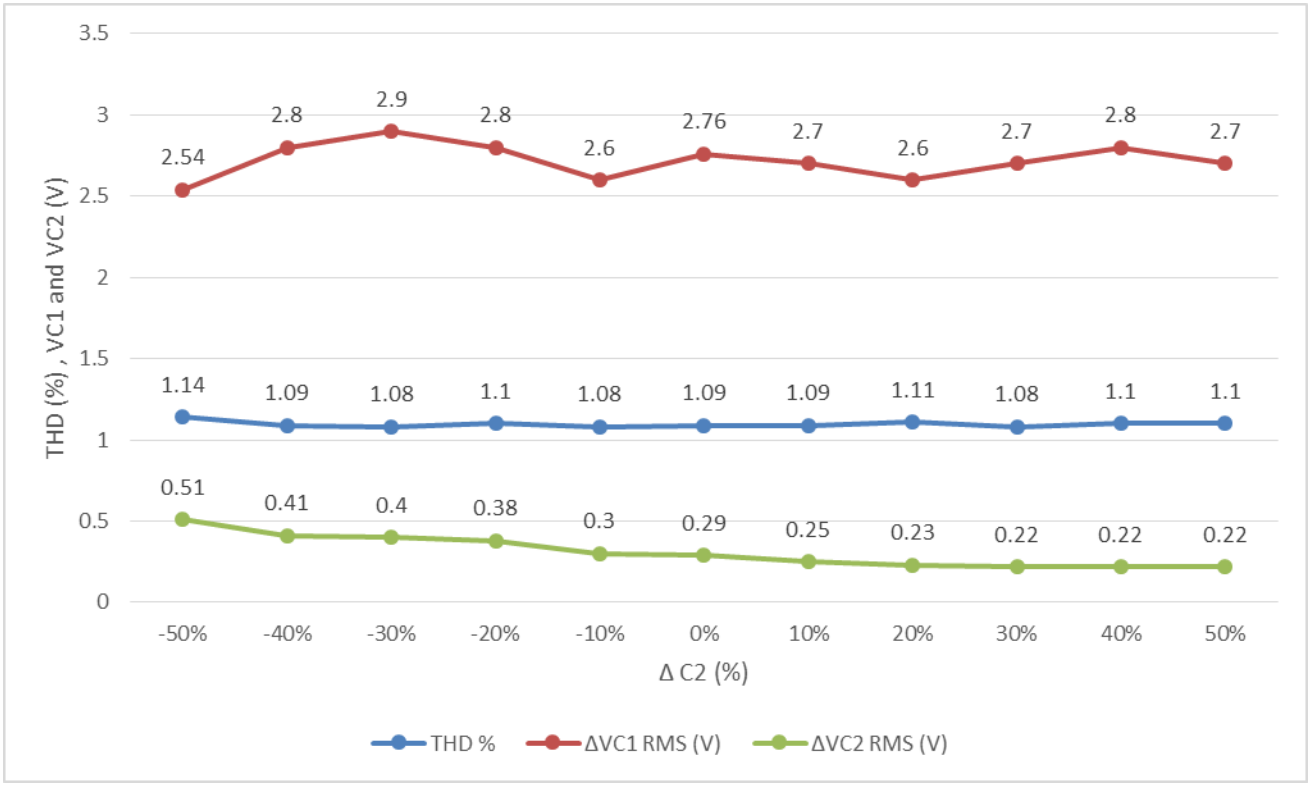


Fig.4. 11: Effect of changing the capacitance of C2on the performance indicators

Figure 4.12 illustrate the effect of changing the inductance of Lf between 50% to 150% of its nominal value. The THD is decreasing from 2.4% to 0.75% (and still relatively small). ΔV_{C1} is fluctuating around 2.7V_{RMS} and there is no great difference and ΔV_{C2} also within the range.

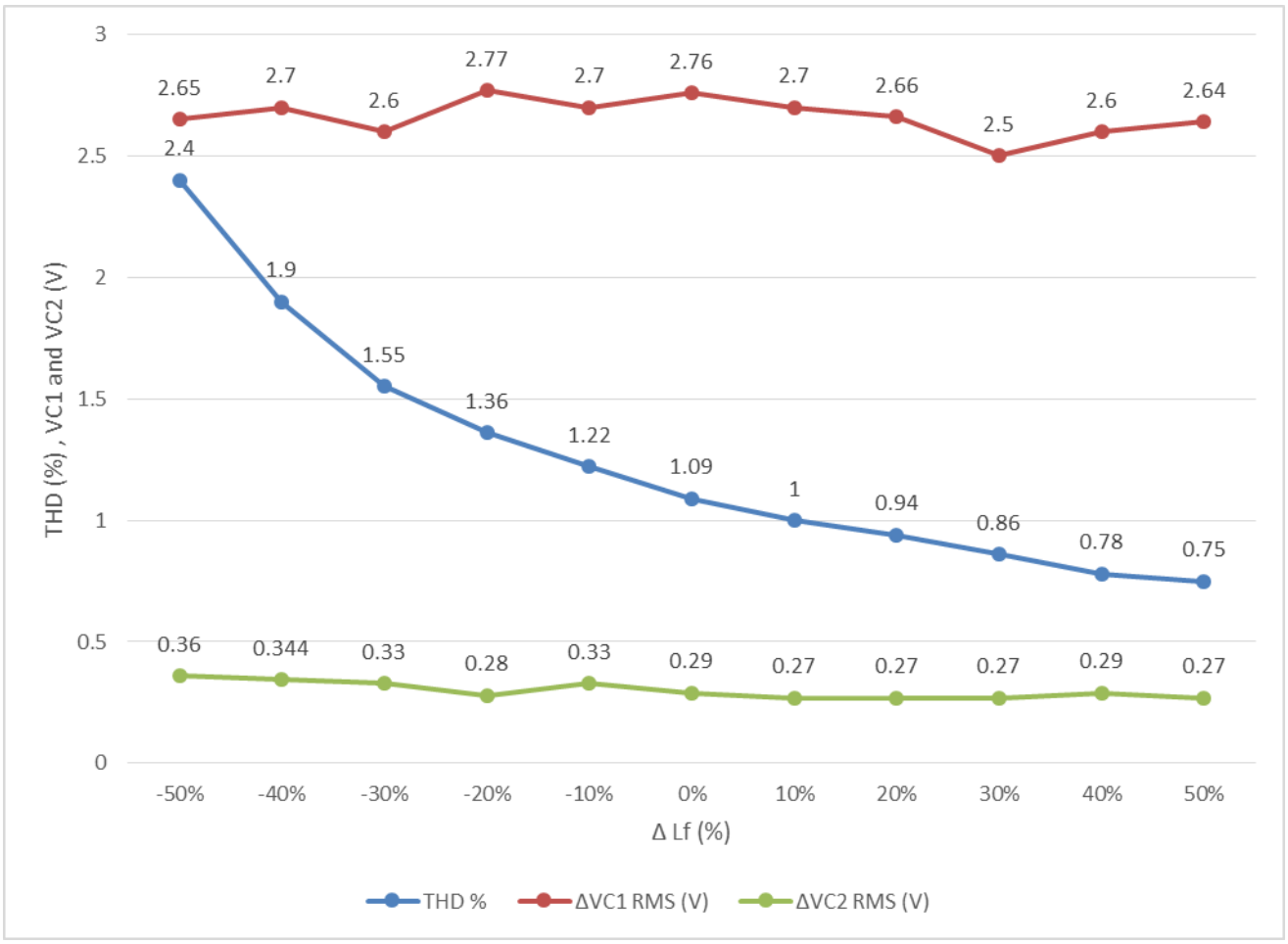


Fig.4. 12: Effect of changing the inductance of Lf on the performance indicators

The effect of grid voltage sag and swell

In order to test the model under grid voltage sag and swell, a step change in the grid voltage has been applied (Vg ± 10%). An increasing of grid voltage by 10% is applied at T=0.7S and decreasing by -10% at T= 0.76S. The model stills robust, the injected current THD have no change and the capacitors' voltages are within the acceptable range.

Fig.4.13 shows how the input voltage changes to follow the grid voltage. Note that the model generates only 7 levels at T= 0.76S due to the decreasing of grid voltage.

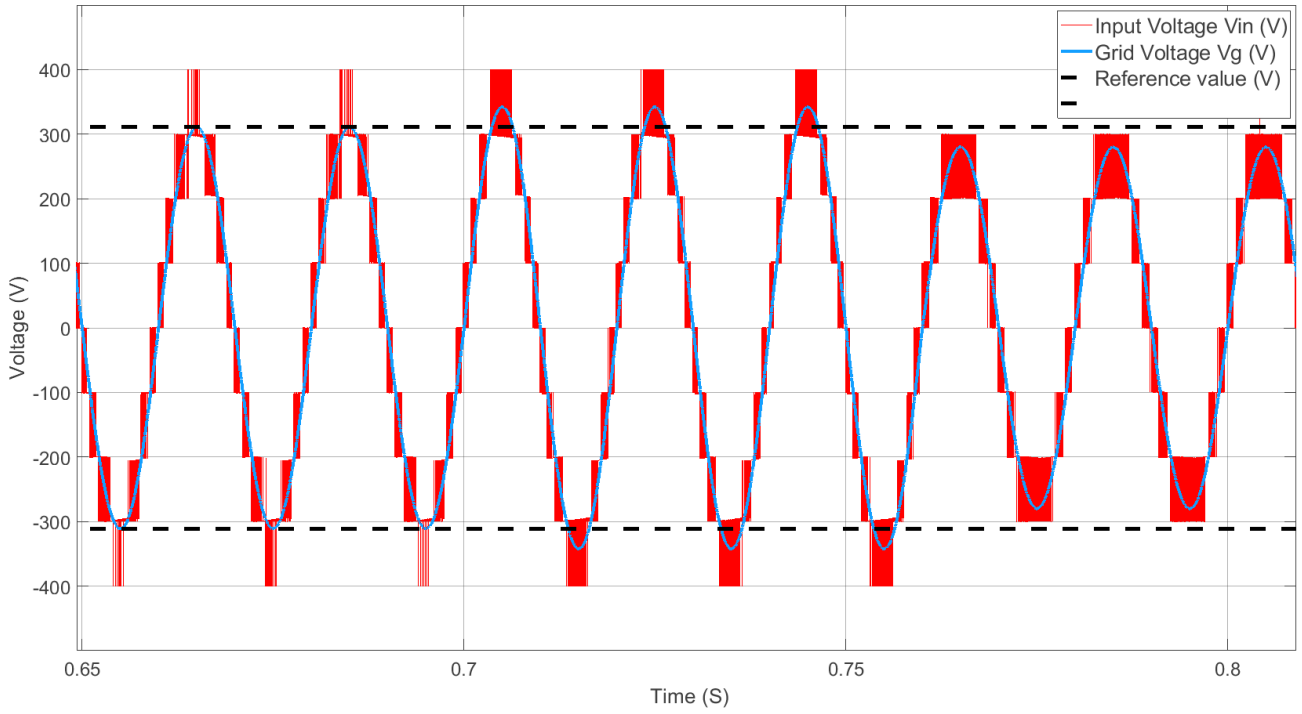


Fig.4. 13: Voltage waveforms of inverter and grid during sag and swell of grid voltage

It's clearly shown from Fig.4.14 that the current injected to the grid has no change due to sag and swell of the grid voltage, the voltage error of C1 has a slight difference but still small and within the acceptable range, the voltage error of C2 has a very slight change and the output power changes due to the difference of the input voltage.

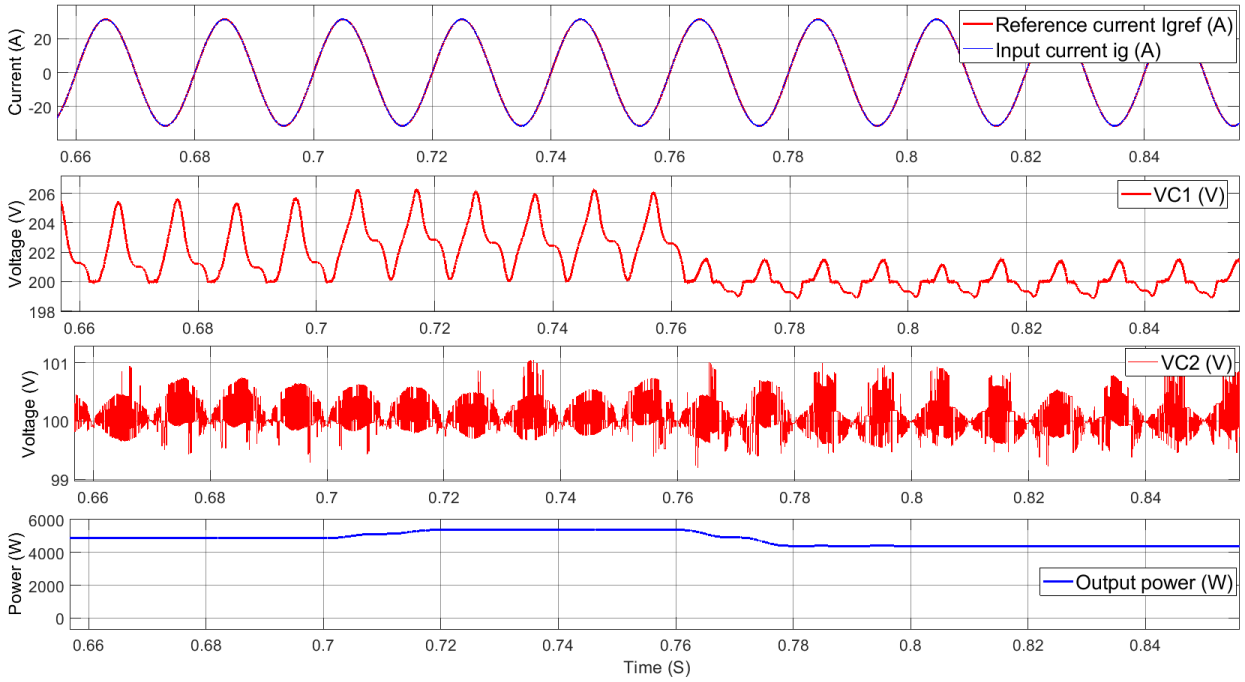


Fig.4. 14: Injected current, VC1, VC2, and output power waveforms during sag and swell of grid voltage

Fig.4.15 illustrates that the injected current error has no change in cases of sag and swell.

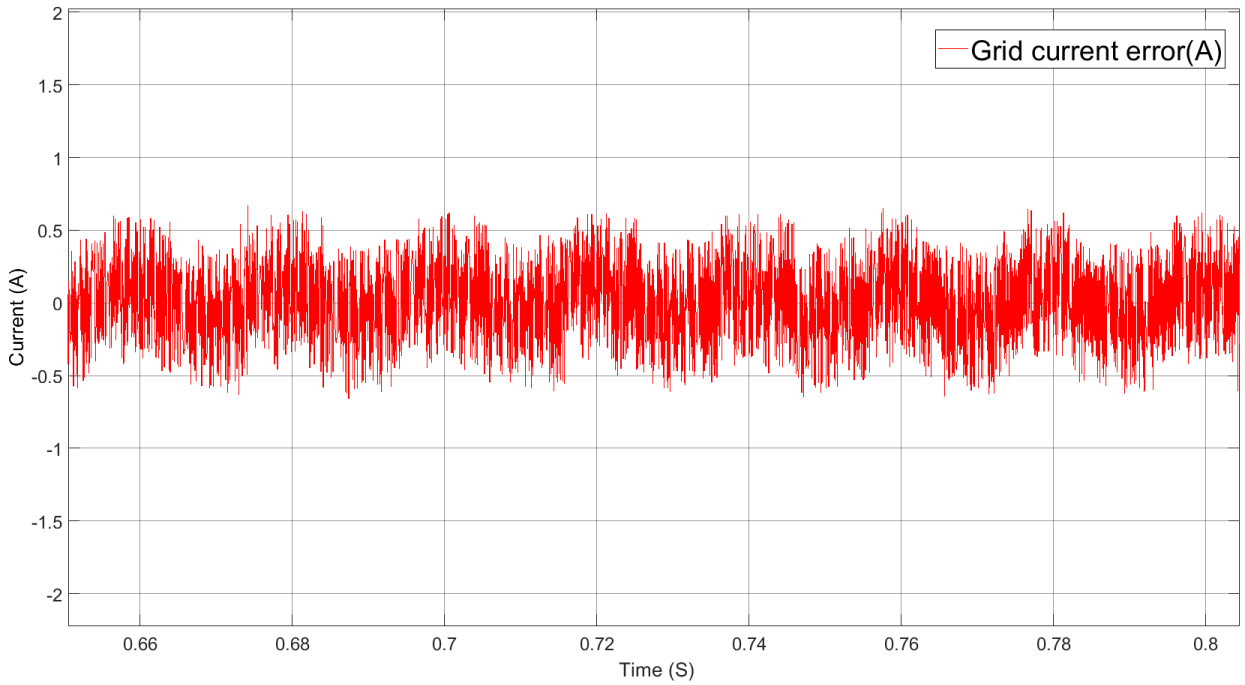


Fig.4. 15 Injected current error sag and swell of grid voltage

CHAPTER FIVE
CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

In this thesis PUC9 multilevel inverter topology controlled by FCS-MPC technique is theoretically analyzed, mathematically modeled and simulated using MATLAB/SIMULINK software.

Simulation results shows that the PUC9 multivariable can be simultaneously controlled by FCS-MPC technique. The weighting factor (α) is tuned successfully based on decreasing THD of the injected current while balancing the capacitors' voltages at their nominal values.

The proposed controller behaves as stable and efficient reference current tracking and has the capability of maintaining the capacitors' voltages at their desired values during steady state and transient response.

The robustness analysis has shown that the step change in the injected current, parameters' mismatching and grid voltage sag and swell does not have a significant effect on the model performance.

5.2 Future work

This study is carried out based on simulation, so this model can be experimentally implemented in order to validate the simulation results.

Also, this topology with 4 pairs of switches can generate 15 different voltage levels, so, by making some changes and using another type of controllers, the distortion of voltage waveform and the stress on switches can be decreased.

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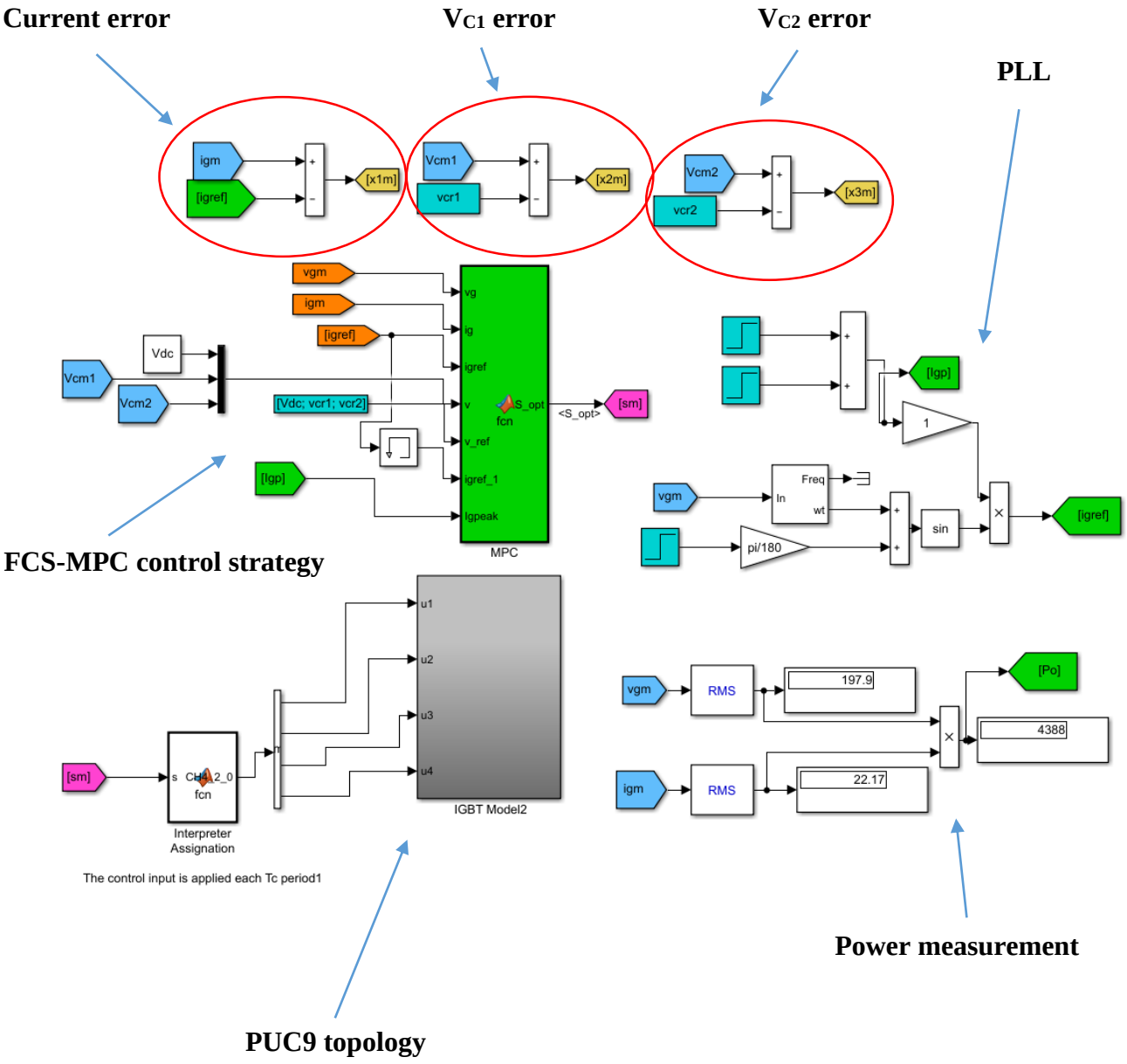
APPENDICES

Appendix A

Matlab/Simulink model



Appendix B

PUC9 topology in MATLAB